CONFIDENTIAL B

MT6765 Design Notice V0.1

2017/11

MT6765 Design Notice Versions

- MT6765 SoC design notice

Category	Description	Date	Version	Remark
BB	Baseband design notice	2017/11/30	V0.1	
BB	Platform dependent design notice	NA	V0.1	For MT6765
BB	Memory (DRAM & eMMC) design notice	NA	V0.1	Common
BB	eFuse design notice	NA	V0.1	Common
BB	SIM design notice	NA	V0.1	Common
BB	LCM design notice	NA	V0.1	Common
BB	Camera design notice	NA	V0.1	Common
BB	USB design notice	NA	V0.1	Common
BB	MEMS sensor design notice	NA	V0.1	Common
BB	SD & eMMC design notice	NA	NA	Common
BB	Capacitive type touch panel design notice	NA	NA	Common
BB	ESD design notice	NA	NA	Common

MT6765 Platform Design Notice

- MT6765 Turnkey solution design notice

Category	Description	
MT6765	MT6765 design notice	WCP > HW > Smart Phone > LTE_6M > MT6765
	MT6765 PCB layout/PDN/MMD/SMT guide	WCP > HW > Smart Phone > LTE_6M > MT6765
	MT6765 SCH and PCB design checklist	WCP > HW > Smart Phone > LTE_6M > MT6765
	MT6357 Co-clock design notice For MT6765	WCP > HW > Smart Phone > LTE_6M > MT6765
PMIC (MT6357/MT6371)	MT6357 PMIC design notice For MT6765	WCP > HW > Smart Phone > LTE_6M > MT6765
	MT6371 Sub-PMIC design notice	WCP > Common IC > PMIC > MT6371
	MT6357 audio & speech design notice For MT6765	WCP > HW > Smart Phone > LTE_6M > MT6765
	MT6357 RTC design notice	WCP > Common IC > PMIC > MT6357
Connectivity (MT6631)	MT6631 design notice	WCP > Common IC > SP Connectivity
RF (MT6177)	MT6177 design notice	WCP > Common IC > RF_LTE
RF (MT6177M)	MT6177M design notice	WCP > Common IC > RF_LTE
Common	Thermal design notice	WCP > HW > Common Design Notes > Thermal
	LTE phone ANT guideline	WCP > HW > Common Design Notes > Anetnna
	NFC design notice	WCP > Common IC > NFC

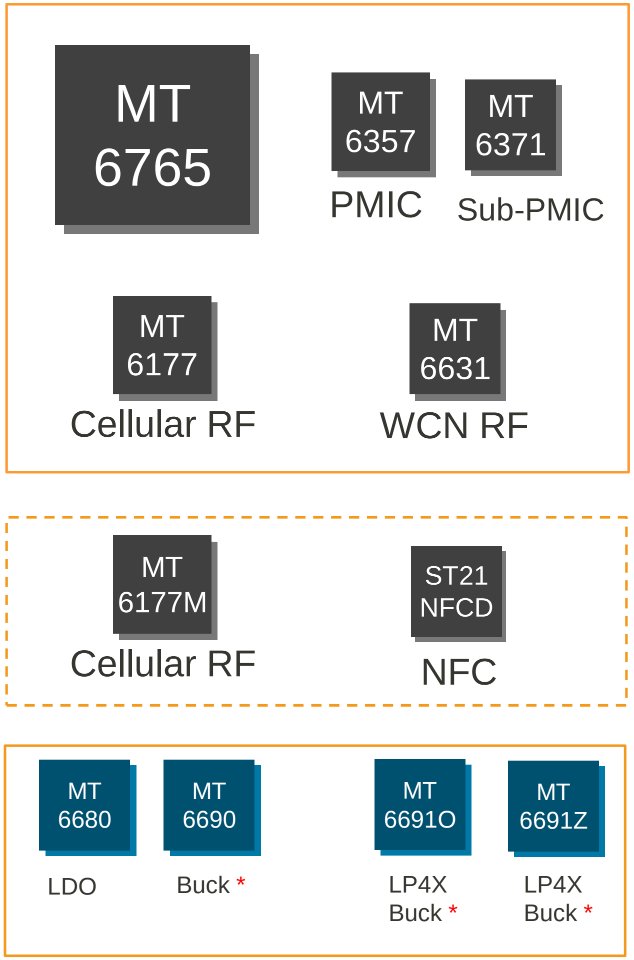
Find the turnkey solution design notices on DCC.

Change List

Version	Date	Description
V0.1	2017.11.23	1. Initial release

Platform High Level introduction

MT6765 Platform Chipset

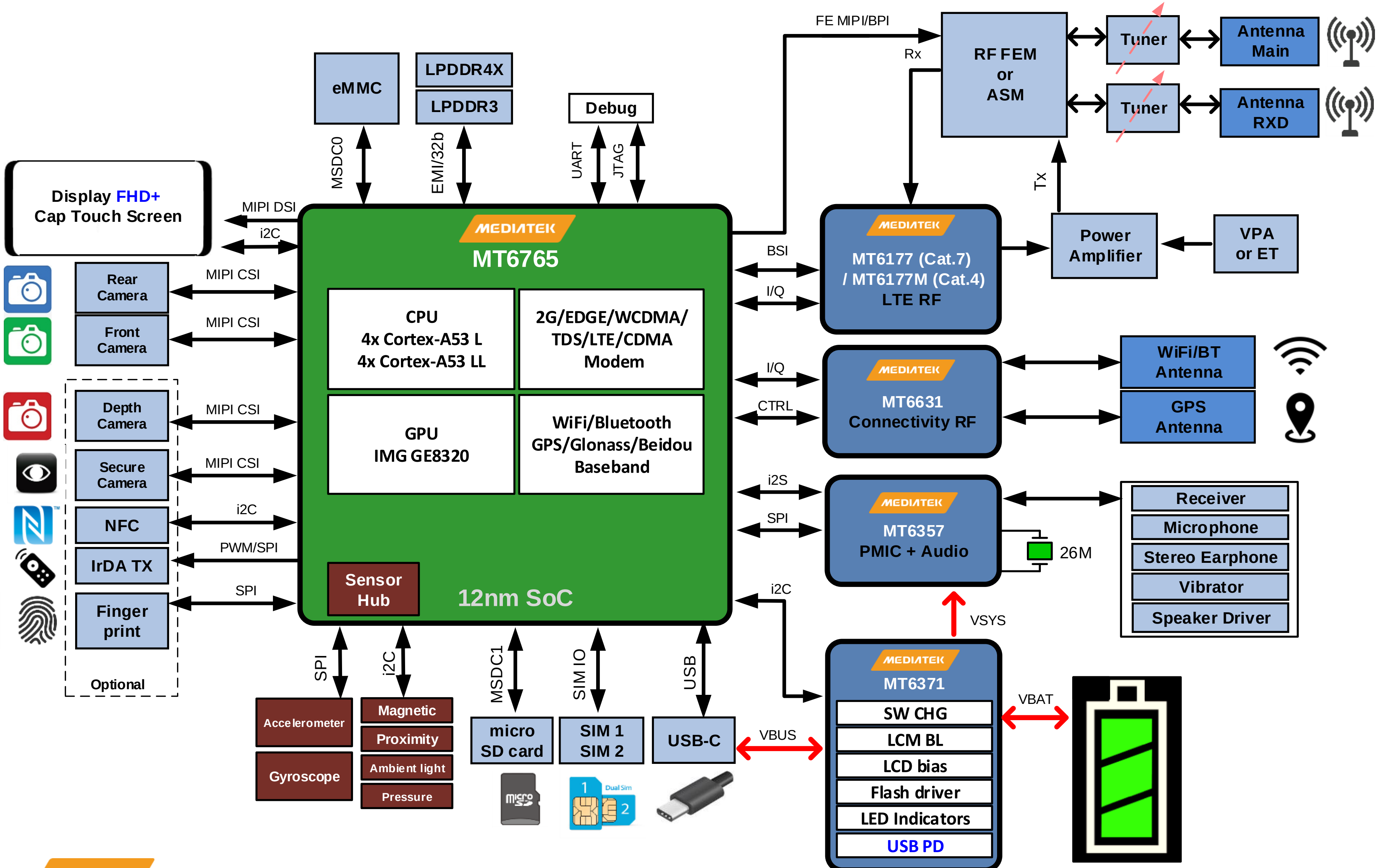


Mediatek Platform		Package size	Type	Pitch	Pin #
BB	MT6765	11 x 11.4 x 0.9	VFBGA	0.4	558
RF	MT6177	5.0 x 5.4 x 0.7	FCCSP	0.4	144
WCN	MT6631	5.0 x 5.0 x 0.9	QFN	0.4	40
PMIC	MT6357	6.6 x 7.0 x 1.0	VFBGA	0.4	209
PMIC	MT6371	4.2 x 4.1 x 0.5	WLCSP	0.4	93

Optional Chips		Package size	Type	Pitch	Pin #
RF	MT6177M	4.6 x 5.0 x 0.87	FCCSP	0.4	120
NFC	ST21NFCD	4.0 x 4.0 x 0.8	WFBGA	0.4	64

* Note : these chipset are subject to change by Marketing, please refer to the latest MT6765-series introduction documents.

MT6765 System Block



MT6765 High-Level Spec Comparisons

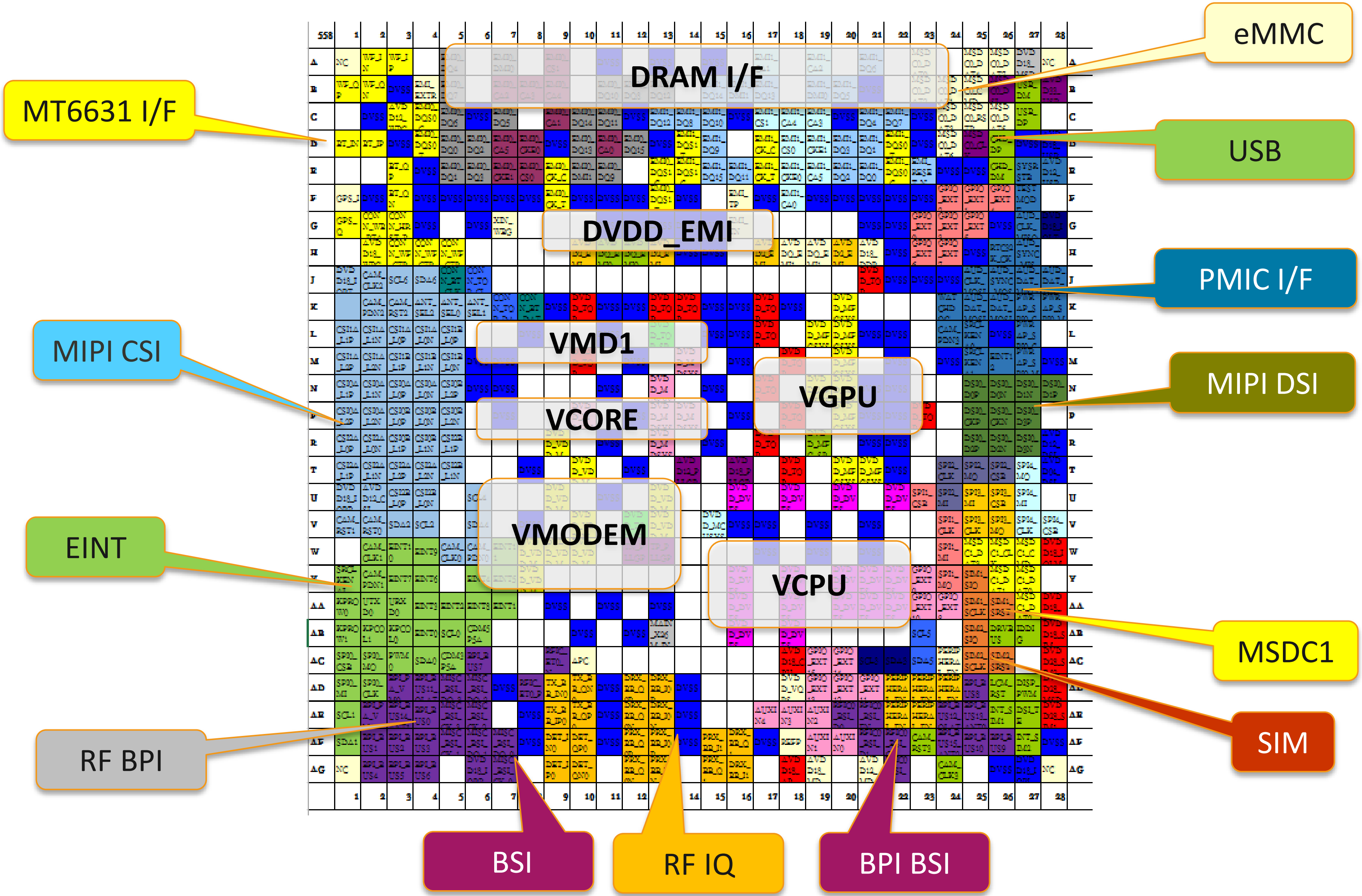
	MT6765	MT6750	MT6763
Process	**12nm**	28nm	16nm
Apps CPU	4xCortex-A53 up to 2.3Ghz * 4xCortex-A53 up to 1.7Ghz *	4xCortex-A53 up to 1.5Ghz 4xCortex-A53 up to 1.0Ghz	4xCortex-A53 up to 2.0Ghz 4xCortex-A53 up to 1.5Ghz
Graphics	**IMG GE8320** **Up to 680Mhz** *	ARM Mali-T860 MP2 Up to 680Mhz	ARM Mali-G71 MP2 Up to 700Mhz
Memory	1xLP3 933MHz, up to 4GB 2xLP4x 1600MHz, up to 6GB eMMC5.1	1xLP3 833MHz, up to 4GB eMMC5.1	1xLP3 933MHz, up to 4GB 2xLP4x 1600MHz, up to 6GB eMMC5.1
Camera	**25MP @ 30fps w/ ZSD** * **13MP + 13MP @ 30fps (LP4X)** * **MIPI Lane : 4+4+4 / 4+4+2+2** **HW Dual cam**	16MP @ 30fps w/ ZSD 13MP + 5MP @ 30fps MIPI Lane : 4+4 SW Dual cam	24MP @ 30fps w/ ZSD 13MP + 13MP @ 30fps (LP4X) MIPI Lane : 4+4 SW Dual cam
Video Dec.	1080p 30fps H.264/H.265	1080p 30fps H.264/H.265	1080p 30fps H.264/H.265
Video Enc.	1080p 30fps H.264	1080p 30fps H.264	1080p 30fps H.264
Display	**FHD+ (2400x1080)** *	FHD (1920x1080)	FHD (1920x1080)
Modem	**Cat-7, L+L**	Cat-6, L+W	Cat-7, L+L
Transceiver	**MT6177 (Cat.7)** **/MT6177M (Cat.4)**	MT6176	MT6177
PMIC	MT6357	MT6353	MT6356
Connectivity	**MT6631** **(+11.ac +BT5.0 +Galileo)**	MT6625L	MT6625L
Sensor Hub	**Yes**	No	No

* Note : these HW capability are subject to change by Marketing, please refer to the latest MT6765-series introduction documents.

Peripherals Comparisons

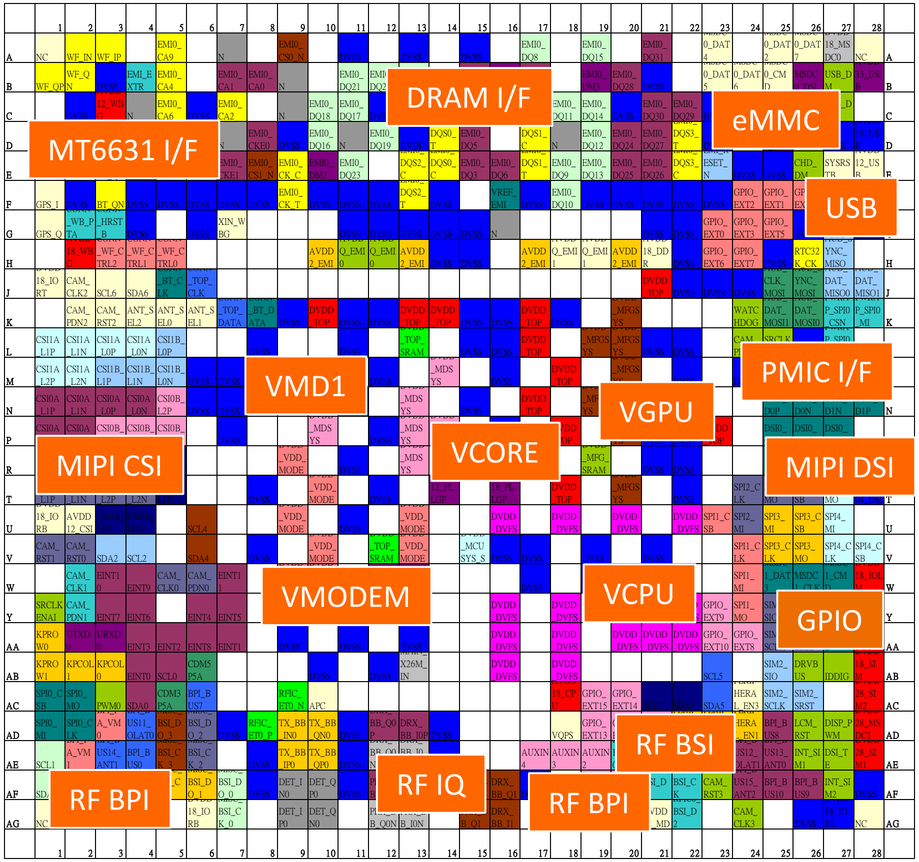
	MT6765	MT6763
USB	USB 2.0	USB 2.0
SDIO	2	2
SPI	6	6
PWM	6	3
UART	2	2
Consumer IR	Supported (TX only)	Supported (TX only)
I2C	**7**	6+1
I2S	4	4
Audio AMP	Not Integrated (ext. solution)	Not Integrated (ext. solution)
AUXADC	5	5
PCM	2	2
DPI	0	1
GPIO	**179**	152

MT6765 Ball Out

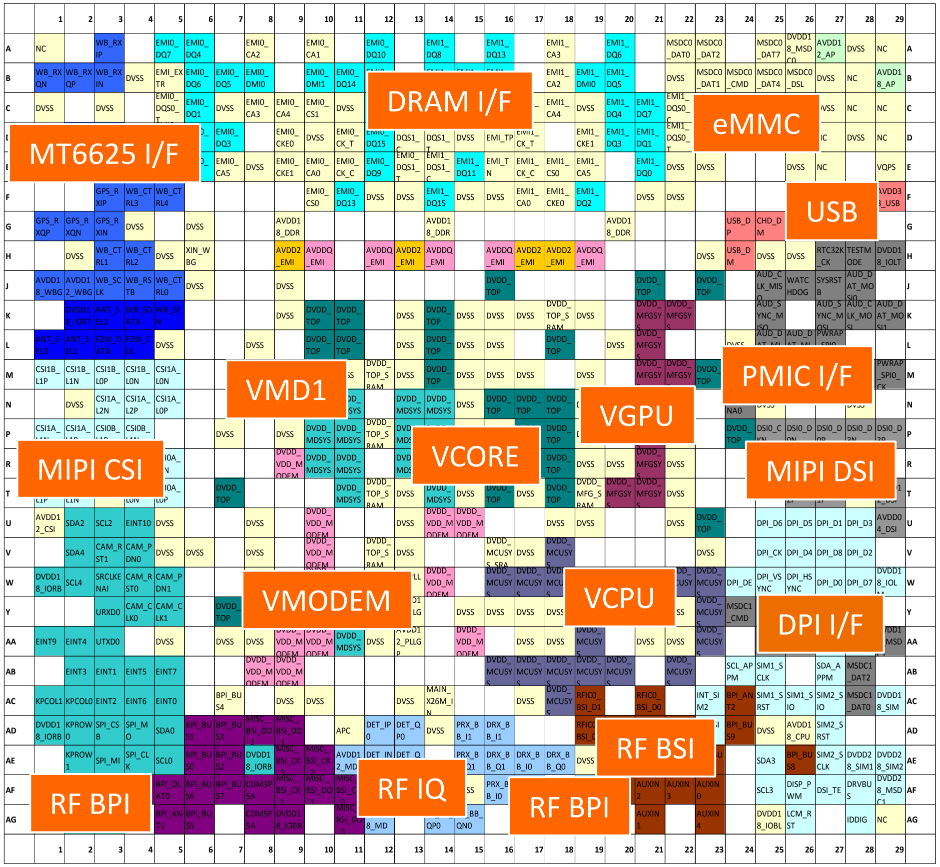


IC Ballout Diff. Table Between MT6765/6763

MT6765 (11mmx11.4mm)

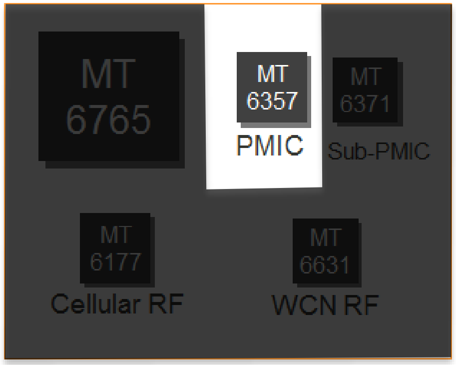


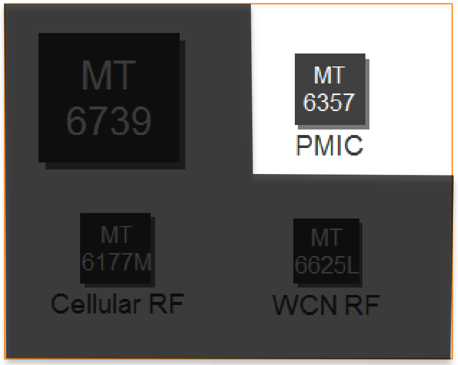
MT6763 (11mmx11.8mm)



PMIC Part Number Notice

SoC	MT6765	MT6739
PMIC	MT6357 **CRV**	MT6357 V



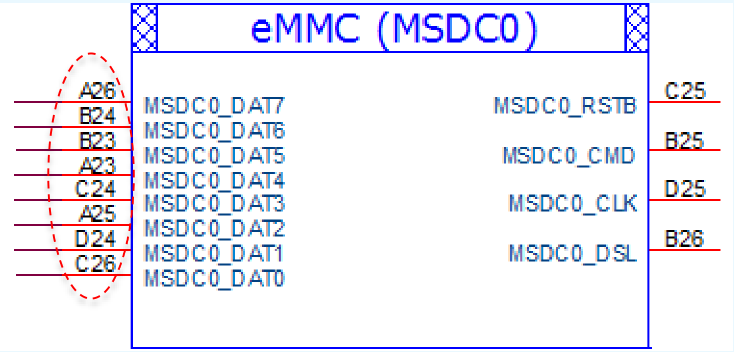
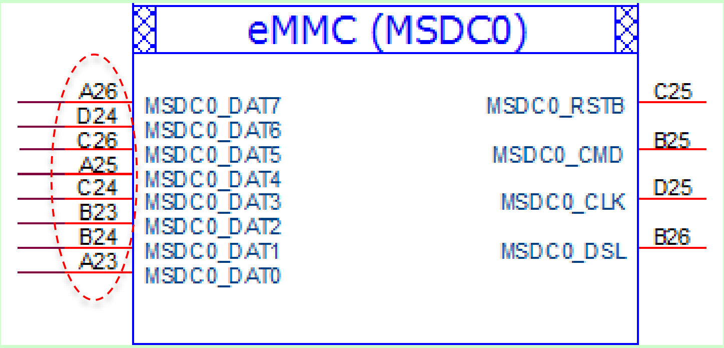


Platform Dependent

Baseband Design Notice

Design Notice: Booting HW trapping

- **Boot mode selection**

<table>
<tr><th></th><th>LPDDR3 eMCP</th><th>LPDDR4X eMCP</th></tr>
<tr><td>HW Trap pin</td><td>PWRAP_SPI0_MI (Pin : K28) : 12K PD</td><td>not required</td></tr>
<tr><td>eMMC DAT[7:0] Pin Out
(schematic)</td><td>
</td><td>
</td></tr>
<tr><td>GPIO Setting
(DCT tool)</td><td>
<table>
<tr><td>GPIO122</td><td>2:MSDC0_CMD</td></tr>
<tr><td>GPIO123</td><td>2:MSDC0_DAT4</td></tr>
<tr><td>GPIO124</td><td>2:MSDC0_CLK</td></tr>
<tr><td>GPIO125</td><td>2:MSDC0_DAT5</td></tr>
<tr><td>GPIO126</td><td>2:MSDC0_DAT2</td></tr>
<tr><td>GPIO127</td><td>2:MSDC0_DAT1</td></tr>
<tr><td>GPIO128</td><td>2:MSDC0_DAT6</td></tr>
<tr><td>GPIO129</td><td>2:MSDC0_DAT0</td></tr>
<tr><td>GPIO130</td><td>2:MSDC0_DAT7</td></tr>
<tr><td>GPIO131</td><td>2:MSDC0_DSL</td></tr>
<tr><td>GPIO132</td><td>2:MSDC0_DAT3</td></tr>
<tr><td>GPIO133</td><td>2:MSDC0_RSTB</td></tr>
</table></td><td>
<table>
<tr><td>GPIO122</td><td>1:MSDC0_CMD</td></tr>
<tr><td>GPIO123</td><td>1:MSDC0_DAT0</td></tr>
<tr><td>GPIO124</td><td>1:MSDC0_CLK</td></tr>
<tr><td>GPIO125</td><td>1:MSDC0_DAT2</td></tr>
<tr><td>GPIO126</td><td>1:MSDC0_DAT4</td></tr>
<tr><td>GPIO127</td><td>1:MSDC0_DAT6</td></tr>
<tr><td>GPIO128</td><td>1:MSDC0_DAT1</td></tr>
<tr><td>GPIO129</td><td>1:MSDC0_DAT5</td></tr>
<tr><td>GPIO130</td><td>1:MSDC0_DAT7</td></tr>
<tr><td>GPIO131</td><td>1:MSDC0_DSL</td></tr>
<tr><td>GPIO132</td><td>1:MSDC0_DAT3</td></tr>
<tr><td>GPIO133</td><td>1:MSDC0_RSTB</td></tr>
</table></td></tr>
</table>

Schematic Notice: Transceiver RX IQ interface

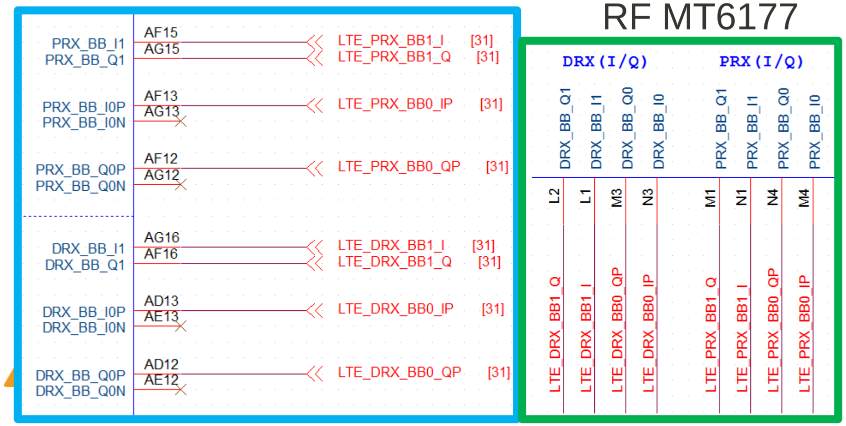
- MT6765 can support RF transceiver MT6177 or MT6177M.
- Please follow the RX IQ connection below.
  - MT6177 RX IQ is single-ended.
  - MT6177M RX IQ is differential.
- For unused IQ pins, do not connect to GND and keep Cap load<5pF.

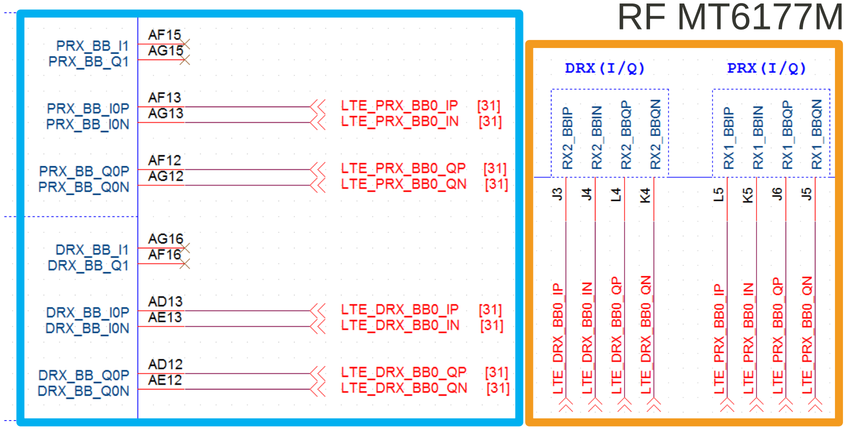
SoC MT6765	
pin no.	pin name
AF15	PRX_BB_I1
AG15	PRX_BB_Q1
AF13	PRXBB_I0P
AG13	PRX_BB_I0N(NC)
AF12	PRX_BB_Q0P
AG12	PRX_BB_Q0N(NC)
AG16	DRX_BB_I1
AF16	DRX_BB_Q1
AD13	DRX_BB_I0P
AE13	DRX_BB_I0N(NC)
AD12	DRX_BB_Q0P
AE12	DRX_BB_Q0N(NC)

RF MT6177	
pin name	pin no.
PRX_BB_I1	N1
PRX_BB_Q1	M1
PRX_BB_I0	M4
PRX_BB_Q0	N4
DRX_BB_I1	L1
DRX_BB_Q1	L2
DRX_BB_I0	N3
DRX_BB_Q0	M3

SoC MT6765	
pin no.	pin name
AF15	PRX_BB_I1(NC)
AG15	PRX_BB_Q1(NC)
AF13	PRXBB_I0P
AG13	PRX_BB_I0N
AF12	PRX_BB_Q0P
AG12	PRX_BB_Q0N
AG16	DRX_BB_I1(NC)
AF16	DRX_BB_Q1(NC)
AD13	DRX_BB_I0P
AE13	DRX_BB_I0N
AD12	DRX_BB_Q0P
AE12	DRX_BB_Q0N

RF MT6177M	
pin name	pin no.
RX1_BBIP	L5
RX1_BBIN	K5
RX1_BBQP	J6
RX1_BBQN	J5
RX2_BBIP	J3
RX2_BBIN	J4
RX2_BBQP	L4
RX2_BBQN	K4





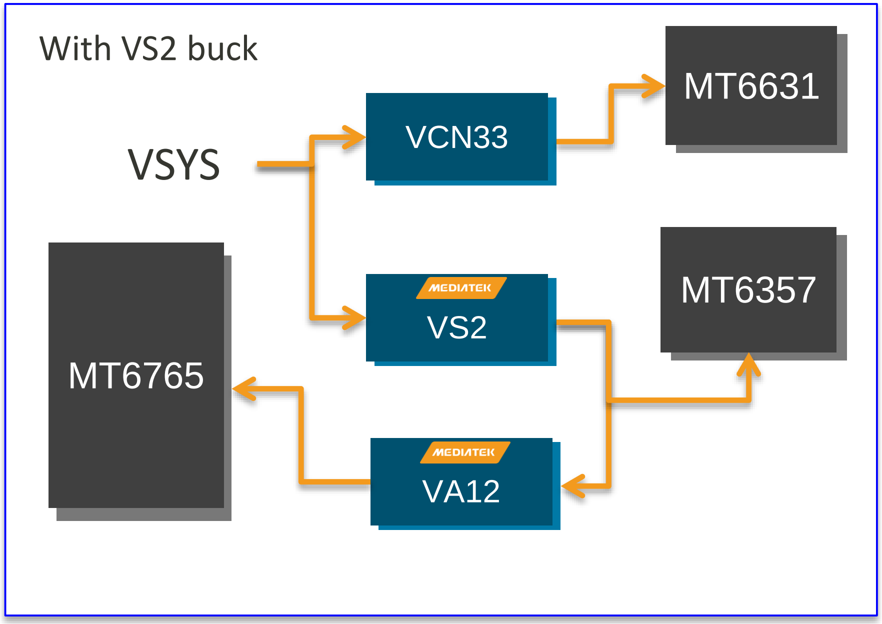
Audio Smart PA Selection Notice

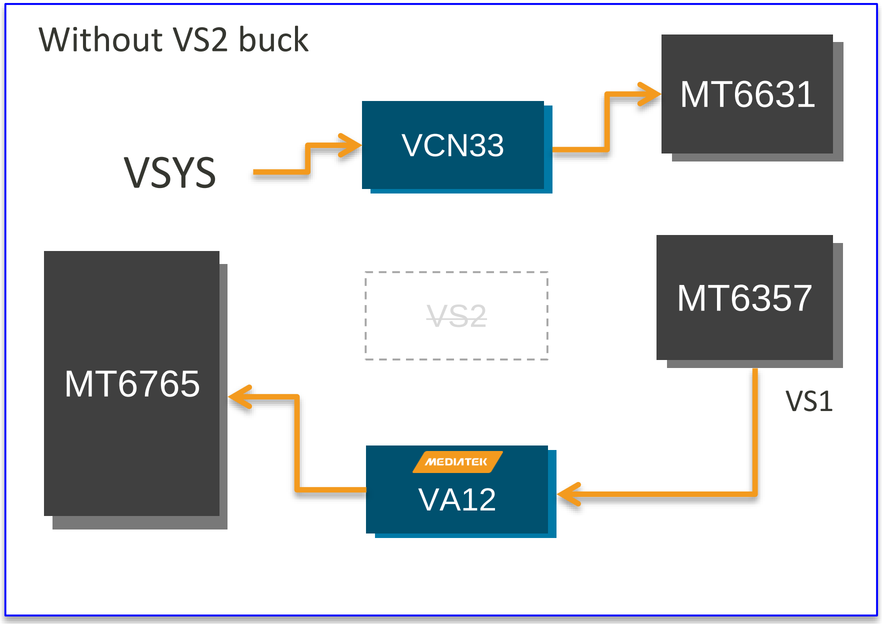
- MT6765 can support Sensor hub and audio Smart PA with below limitation
- Select audio Smart PA hardware, also considering with Sensor Hub feature

Selection	**Sensor Hub** (Software option)	**Audio Smart PA** (Hardware component)	**MT6765 Support**
Option 1	software disable	with DSP (ex: RT5509)	Yes
Option 2	software Enable	with DSP (ex: RT5509)	Yes
Option 3	software disable	without DSP (ex: RT5510)	Yes
Option 4	software Enable	without DSP (ex: RT5510)	**Not support**

Schematic Notice: External Power

- MT6765 Platform require external power as below (e.g. not include by PMIC)
  - VS2 Buck (optional, low power performance trade-off)
  - VA12 LDO (must)
  - VCN33 LDO (must)





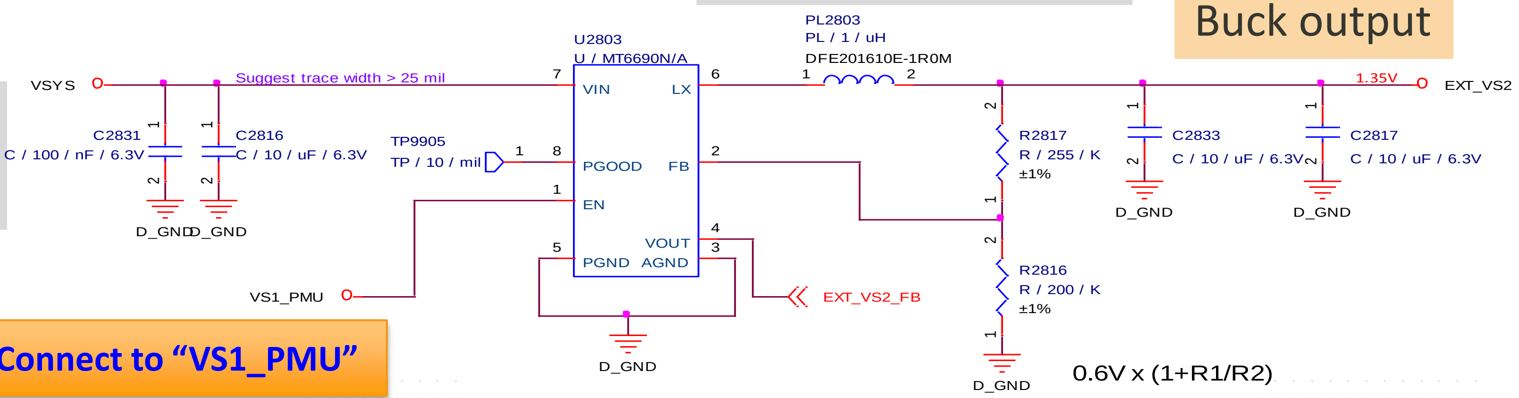
Ext. Power Requirement : VS2

- VS2 Ext Buck Reference : MT6690N/A
- Voltage Output: 1.35V
- Current Output: 2A
- Reference Schematic:

LX should be connected to inductor by wide and short trace. Keep sensitive components away from this trace.

Buck output

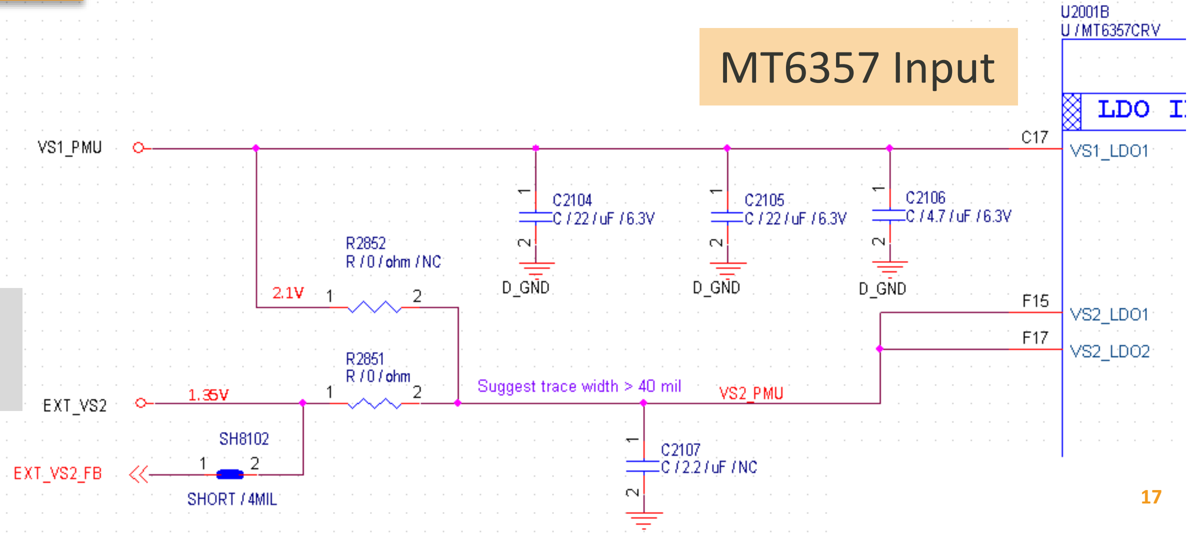
Input cap (C_{in}) must be placed as close to the IC Vin pin as possible. This capacitor provides the AC current into the internal power MOSFETs.



EN pin Connect to "VS1_PMU"

0.6V x (1+R1/R2)

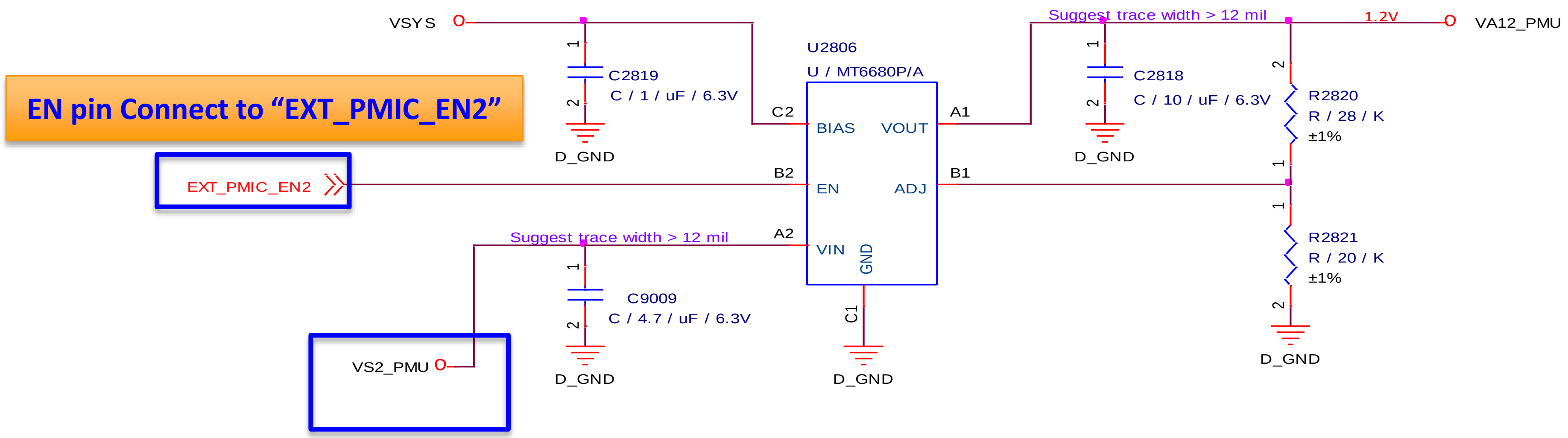
MT6357 Input



The Feedback must be connected as close to the device as possible. Layout trace using GND shielding to avoid noise coupled. Also avoid to overlap with noisy source like LX / CLK in layer N+1 & N-1.

Ext. Power Requirement : VA12

- VA12 Ext LDO Reference: MT6680P/A
- Voltage Output: 1.2V
- Current Output: 1A
- For better efficiency, VA12 input recommend to connect **“Ext VS2 1.35V”**
  - If VS2 external buck is absence, connect VA12 input to “PMIC VS1 2.1V” instead
- Reference Schematic:



- **With VS2 buck : Vin connect to EXT VS2 1.35V Vout**
- **Without VS2 buck : Vin connect to PMIC VS1 2.1V Vout**

Ext. Power Requirement : VCN33

- Input voltage range: **3.4V-5.0V**
- Output current capability: **1A at least**
- Output Voltage : **3.3V**
- Voltage accuracy spec:
  - **DC : ±1%**
  - **AC : ±4%**
  - ✓ **AC Transient current profile**

    - 1mA->9mA (0.1uS slew rate)

    - 6mA->100mA (0.5uS slew rate)

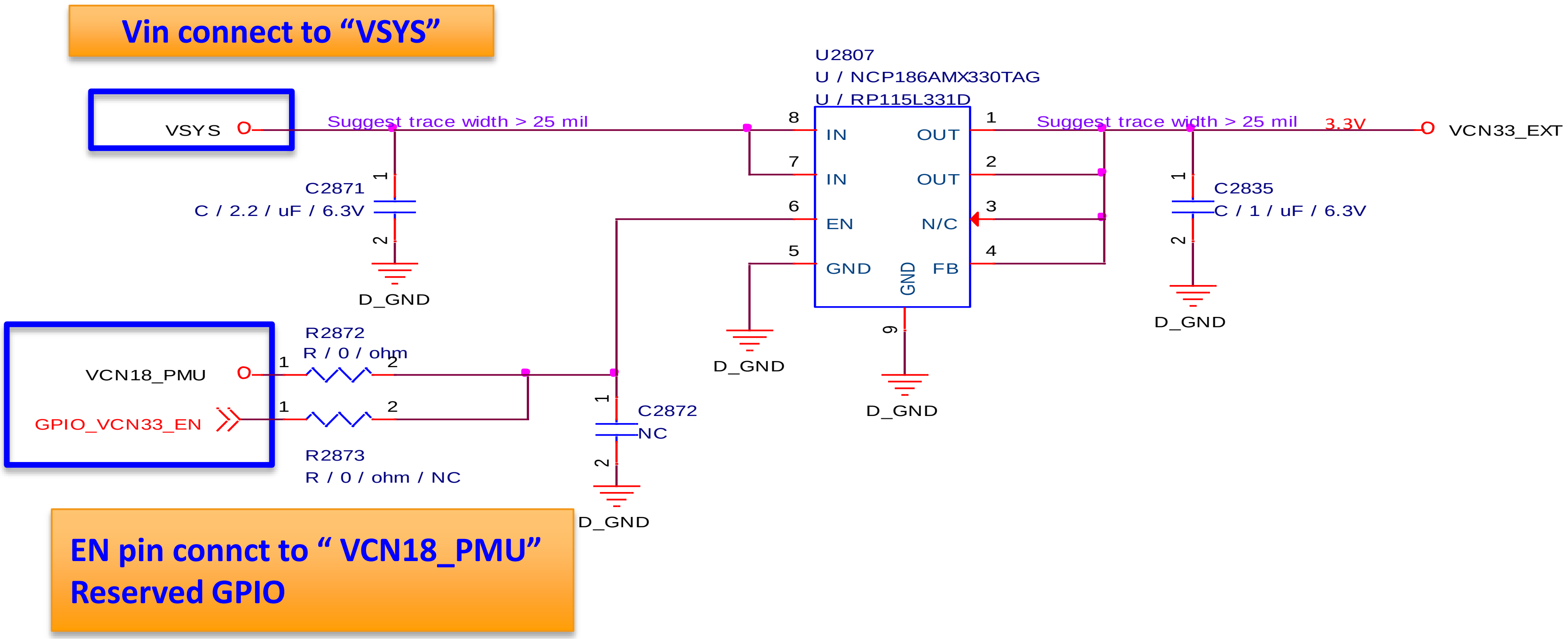
    - 90mA->480mA (0.2uS slew rate)

    - 480mA-> 1A (2uS slew rate)

- Power Sequence Requirement
  - **Please connect EN pin to main PMIC "VCN18_PMU" and reserved GPIO connection**
  - **Power Off need discharge function for Fast discharge power down**

Ext. Power Requirement : VCN33

- VCN33 Ext LDO Reference : NCP186AMX330TAG / RP115L331D
- Voltage Output: 3.3V
- Current Output: 1A
- Reference Schematic:



Generic Interface and Peripheral Design Notice

Design Notice: i2C/i3C Application (1/3)

Set	Controller	Ref. design	Note
I2C-0	AP	Cap Touch Controller	1. Push-pull type 2. Open drain type -- Fast mode 400KHz
I2C-1(I3C)	AP Sensor Hub	MEMS sensors*	1. Push-pull type 2. Open drain type -- Fast mode 400KHz
I2C-2(I3C)	AP	Rear camera	1. Push-pull type 2. Open drain type -- Fast mode 400KHz
I2C-3	AP	NFC Audio Smart PA	1. Push-pull type 2. Open drain type -- Fast mode 400KHz
I2C-4(I3C)	AP	Front camera	1. Push-pull type 2. Open drain type -- Fast mode 400KHz
I2C-5	AP	Sub-PMIC MT6371	1. Push-pull type 2. Open drain type -- Fast mode 400KHz
I2C-6	AP	Reserved	1. Push-pull type 2. Open drain type -- Fast mode 400KHz

- A few cameras may lock I2C bus due to large leakage in power off mode. We suggest you use dedicated I2C bus for those cameras.
- I2C address must be unique for the devices shared with the same I2C bus.
- If the camera supports PIP/VIV feature, and AF driver IC is the same, assign different I2C bus for the front camera.
- For standard mode / Fast mode, recommend using open drain type (HW default internal pull-up 5KΩ, SW initial change to internal pull-up 1KΩ)
- For fast mode plus / High speed mode, recommend using Push-pull type

* Refer to MEMS Sensor interface connection

Design Notice: i2C/i3C Application (2/3)

- MT6765 integrates 7 i2C controllers: I2C-0, I2C-1, I2C-2, I2C3, I2C-4, I2C-5, I2C-6

- all i2C are dedicate pins.

Pin name	Controller	Pin num	IO type	GPIO aux mode
SCL0	I2C-0	GPIO83	Push-pull	Aux Func.1
SDA0		GPIO82		Aux Func.1
SCL1	I2C-1	GPIO84	Push-pull	Aux Func.1
SDA1		GPIO81		Aux Func.1
SCL2	I2C-2	GPIO103	Push-pull	Aux Func.1
SDA2		GPIO104		Aux Func.1
SCL3	I2C-3	GPIO50	Push-pull	Aux Func.1
SDA3		GPIO51		Aux Func.1
SCL4	I2C-4	GPIO105	Push-pull	Aux Func.1
SDA4		GPIO106		Aux Func.1
SCL5	I2C-5	GPIO48	Push-pull	Aux Func.1
SDA5		GPIO49		Aux Func.1
SCL6	I2C-6	GPIO161	Push-pull	Aux Func.1
SDA6		GPIO162		Aux Func.1

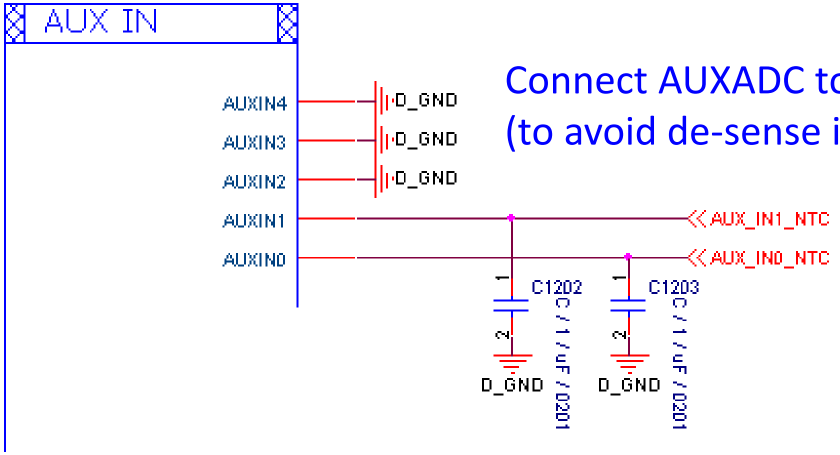
Design Notice: i2C/i3C Application (3/3)

- **I2C / I3C IP Structure**
  - MT6765 integrates 7 I2C controllers : I2C-0, I2C-1, I2C-2, I2C3, I2C-4, I2C-5, I2C-6
  - **I2C1, I2C2, I2C4 support I3C SDR mode only.**
  - The I2C0~I2C6 have the internal pull up 1Kohm, there is no need to add the external pull up resistor. Recommend reserve the NC resistor.
  - For standard mode / Fast mode, recommend using open drain type (HW default internal pull up 5KΩ, SW initial change to internal pull up 1KΩ)
  - For fast mode plus / High speed mode, recommend using Push-pull type
- **I2C / I3C Inter-connection**
  - I3C only Support SDR Mode; Must not connect to HDR-DDR, HDR-TSP and HDR-TSL Modes Only devices.
  - The I2C devices must have 50ns spike filter, when the bus have I3C device in I3C SDR mode.
  - I2C / I3C not support the clock stretching when using Push Pull type.
  - A few cameras may lock I2C bus due to large leakage in power off mode. Recommend use dedicated I2C bus for cameras.
  - I2C address must be unique for the devices shared with the same I2C bus.
  - If the camera supports PIP/VIV feature, Rear camera and Front camera Must use separated I2C whether AF driver/sensor driver/EEPROM's I2C slave address are the same or not
  - If the camera supports Dual Camera feature, 1st Rear and 2nd Rear Must use separated I2C whether AF driver/sensor driver/EEPROM's I2C slave address are the same or not
  - If using the Sensor-hub, do not share the SCP I2C Bus to no-sensor type device.

Design Notice: Auxiliary ADC (1/2)

- **MT6765 has x5 AUXADC channels**
  - 5 auxiliary ADC channels (AUXIN[4:0])
  - Supports max. 1.45V input range

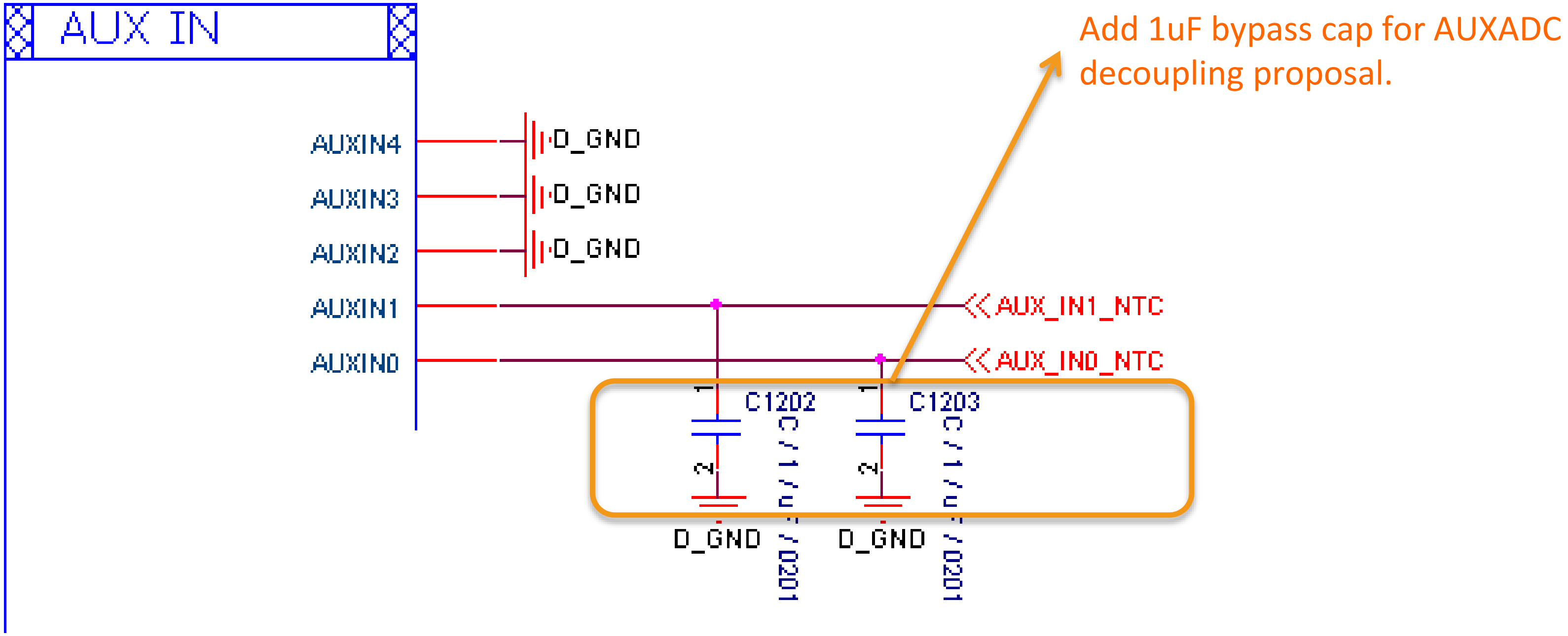
ADC	IO power domain	Dedicate pin	Input range	Resolution	Sampling rate
AUXIN0	AVDD18_AP	V	0.05 ~ 1.45V	12-bit	3.25/(N+4) MSPS @ N-bit
AUXIN1	AVDD18_AP	V	0.05 ~ 1.45V	12-bit	
AUXIN2	AVDD18_AP	V	0.05 ~ 1.45V	12-bit	
AUXIN3	AVDD18_AP	V	0.05 ~ 1.45V	12-bit	
AUXIN4	AVDD18_AP	V	0.05 ~ 1.45V	12-bit	



Connect AUXADC to ground when not in use (to avoid de-sense issues)..

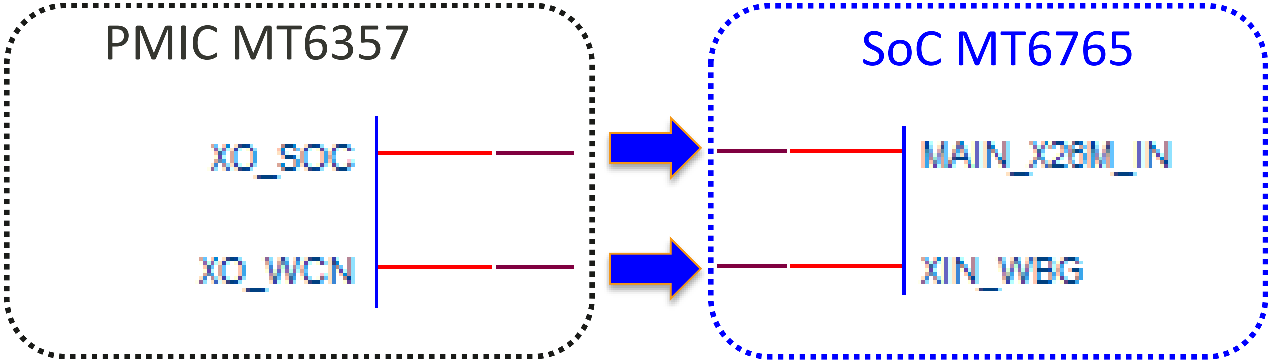
Design Notice: Auxiliary ADC (2/2)

- **AUXADC suggest to add decouple cap.**
  - Add bypass cap near AP when using the AUX_ADC pin for decoupling RF noise
  - If all AUX_ADC ports are not used as ADC, you **can not** use all of them as GPI or EINT function

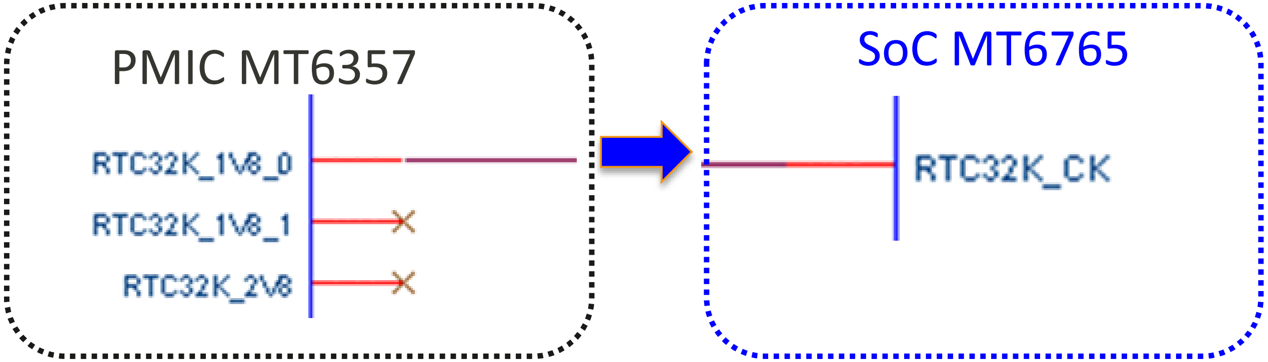


Design Notice: Clock Input

- 26M clock input is DC-coupled (no need capacitor in series connection)



- "RTC32K_CK" (1.8V) 32kHz input is driven by PMIC's "RTC32K_1V8_0".



Design Notice: PWM

- MT6765 have x6 PWM controller (PWM[0:5])
  - PWM supports “Old mode” and “FIFO mode”
    - PWM clock source selection:

Mode	OLD_MODE	CLKSEL_OLD	CLKSEL	CLKSRC
Old mode	1	Don’t care	0	bclk [1]
Old mode	1	0	1	bclk/1625
FIFO mode	0	Don't care	0	bclk
FIFO mode	0	Don't care	1	bclk/1625
Note 1: The bclk can be selected as 26MHz or 68.25MHz				

    - PWM output frequency and duty cycle (%):

Mode	Duty cycle	Output frequency
Old mode	PWM_THRESH / (PWM_DATA_WIDTH + 1)	SRCLK / (CLK_DIV * (PWM_DATA_WIDTH + 1))
FIFO mode	Output freq. = (SRCLK * duty cycle) / 4 ; where the unit of duty cycle is % (percentage).	

  - Detailed PWM pin location, please refer to “MT6765_GPIO_Formal_Application_Spec”
- MT6765 has x1 dedicated CABC PWM controller: DISP_PWM
  - PWM frequency
    - 26M/(PWM_CLKDIV + 1)/1024
    - 104M/(PWM_CLKDIV + 1)/1024
  - PWM duty cycle range: 0% ~ 100%; 1,024 steps
- MT6765 PWM not support working in sleep mode

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Design Notice: CLKM

- CLKM[0:3] can output clock for external application.
  - Only 32k clock output can exist in suspend mode.
  - See the table below for available clock sources.
  - Supports clock divider (/1, /2, /4, /8, /16… /256) but does not guarantee duty

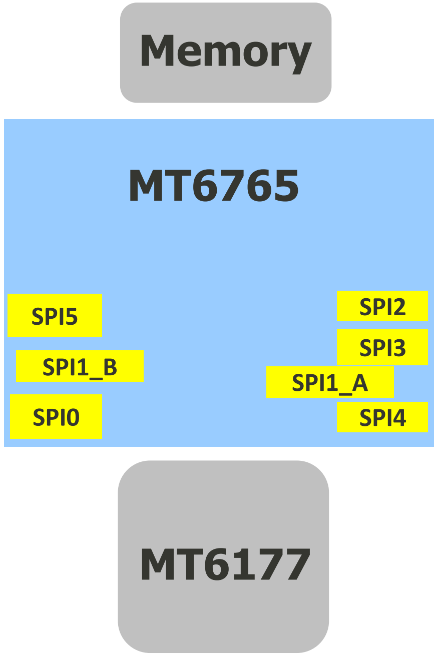
Clock source of CLKM[0:3]	Note
32kHz	
26MHz	
156MHz	
178.3MHz	
196.608MHz	

Note: CLK out frequency will not be changed by SSC (spread spectrum clock) or hopping.

Design Notice: SPI

- MT6765 supports x6 HW SPI ports
  - Max. data rate: 27M bit/s
  - Min. data rate : 0.8K bit/s
  - Both TX/RX support DMA mode.

SPI Port	IO Level	Dedicate Pin	Max. clock rate	Default application
SPI0	1.8V	V	27MHz	Generic device, eSE
SPI1	1.8V	V	27MHz	Generic device
SPI2	1.8V	V	27MHz	Generic device
SPI3	1.8V	V	27MHz	Generic device
SPI4	1.8V	V	27MHz	Generic device
SPI5	1.8V	Pin mux	27MHz	Generic device



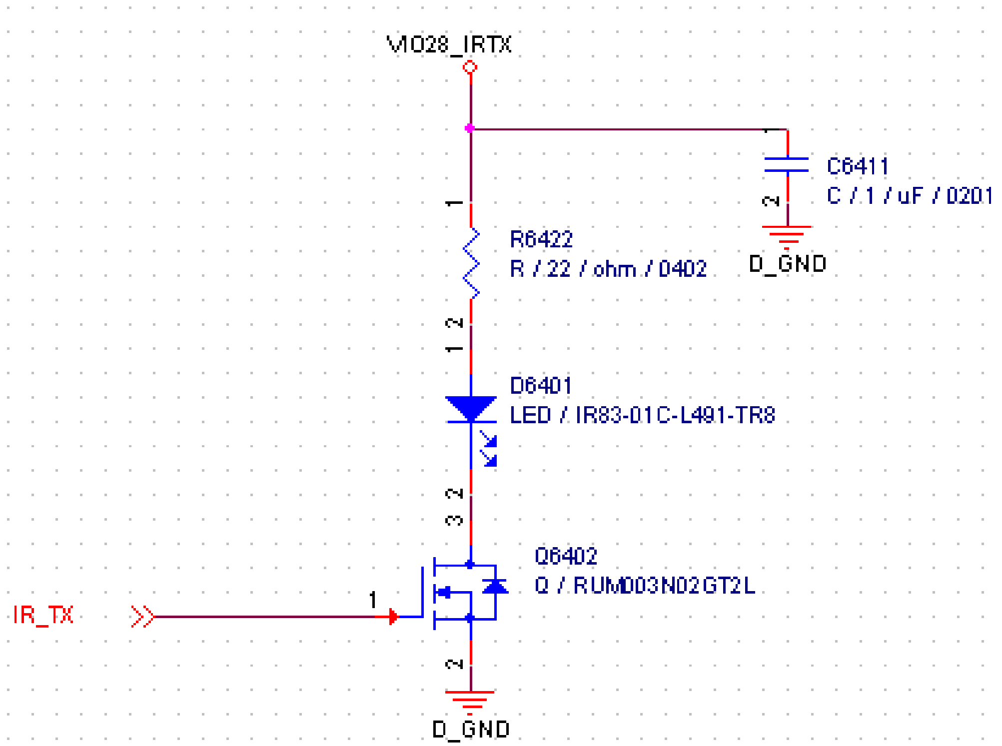
- ** For Fingerprint application, suggest to choose SPI 0/1/5
- ** For Sensor hub application, refer to MEMS Sensor interface connection

Design Notice: IR_TX only (1/3)

- **IR_TX function: Choose pin mux with O:PWM0/1/2/3/4/5**

Signal	Type	Aux Func.
IR_TX	PWM	O: PWM_0/1/2/3/4/5

PWM_0/1/2/3/4/5



Design Notice: IR_TX only (2/3)

- **Component choice and IR_TX distance**
  - **Q6402(N-MOSFET)**
    - Low on-resistance
    - Low voltage drive (1.8V) makes this device ideal for portable equipment
  - **D6401 (IR_LED)**

品名	Dimension(mm)	Wavelength	Intensity	view angle
IR83-01C/L491/TR8	1.6 x 0.8 x 1.52	940nm	4mW/sr at 20mA	X100/Y40deg

  - **IR_TX distance(Note1)**

Summary		
	Value	**Value**
R6422	**6.8 ohm**	**22 ohm**
Q6402(NMOS)	**RUM003N02 (1.8V)**	**RUM003N02 (1.8V)**
D6401(IR_LED)	**IR83-01C-L491-TR8**	**IR83-01C-L491-TR8**
IR TX distance	**Around 9m**	**Around 4m**

Design Notice: IR_TX only (3/3)

- **Component choice and IR_TX distance**
  - **Note1**
    - If customers choose different type of N-MOSFET and IR_LED, need to adjust the value of (R6422) resistance to gain the best distance(Note2,3,4)
  - **Note2**
    - Duty cycle of IRTX_OUT: Default is 33%
      - In this case, the Peak Forward Current of IR_LED(IR83-01C-L491-TR8) should not exceed 300mA
  - **Note3**
    - If customers choose different type of IR_LED, need to ask vendor to provide the “peak forward current” for 33% of duty cycle
  - **Note4**
    - To avoid violating the Absolute Maximum Current Rating of LDO and IR_LED

Design Notice: MSDC Application

Set	Function	Power domain	Note
MSDC0	eMMC	DVDD18_MSDC0	1. Dedicated pin for eMMC 2. Independent power domain
MSDC1	T-card	DVDD28_MSDC1	1. Dedicated pin for T-card 2. Independent power domain

	MT6765 MT6357	Unit
VEMC	3.0	V
VIO18	1.8	V
VMCH	3.0	V
VMC (SD3.0)	1.86	V
VMC (SD2.0)	3.0	V

Design Notice: Debug

- Debug interface
  - Legacy JTAG (reserve TCK and TMS for serial JTAG)
  - AP UART
  - MD UART[0:1] (PinMux)

Interface	AP	MD (L/W/T/G)
Legacy parallel JTAG	V	V
Serial JTAG	V	V
AP UART (UART0)	V	
MD UART[0:1] (pin mux)		V

Design Notice: JTAG HW Trapping Table

- JTAG trapping pin
  - PWRAP_SPI0_CSN, default pull-up (75Kohm typically in SoC)
  - AUD_DAT_MOSI0, default pull-down (75Kohm typically in SoC)
  - For external pull purpose, suggest to use 12Kohm or less
- JTRSTn must be connected

MT6765 Ball name	PWRAP_SPI0_CSN = H AUD_DAT_MOSI0 = L	PWRAP_SPI0_CSN = H AUD_DAT_MOSI0 = H	PWRAP_SPI0_CSN = L AUD_DAT_MOSI0 = L	PWRAP_SPI0_CSN = L AUD_DAT_MOSI0 = H
SPI3_MI	GPIO21	B1:DAP_MD32_SWD		
SPI3_CSB	GPIO22	I0:DAP_MD32_SWCK		
SPI3_CLK	GPIO24	I0:IO_JTAG_TCK		
SPI1_MI	GPIO25	B1:IO_JTAG_TMS		
SPI1_CSB	GPIO26	I1:IO_JTAG_TDI		
SPI1_MO	GPIO27	O:IO_JTAG_TDO		
SPI1_CLK	GPIO28	I1:IO_JTAG_TRSTN		
MSDC1_CLK	MSDC1_CLK			I0:JTCK_SEL2
MSDC1_CMD	MSDC1_CMD			B1:JTMS_SEL2
MSDC1_DAT0	MSDC1_DAT0			I1:JTDI_SEL2
MSDC1_DAT2	MSDC1_DAT2			I1:JTRSTn_SEL2
MSDC1_DAT1	MSDC1_DAT1			O:JTDO_SEL2
SPI0_MI	GPIO155	O:JTDO_SEL1	O:JTDO_SEL1	
SPI0_CSB	GPIO156	B1:JTMS_SEL1	B1:JTMS_SEL1	
SPI0_MO	GPIO157	I1:JTDI_SEL1	I1:JTDI_SEL1	
SPI0_CLK	GPIO158	I0:JTCK_SEL1	I0:JTCK_SEL1	
EINT8	GPIO8	I1:JTRSTn_SEL1	I1:JTRSTn_SEL1	

MD JTAG

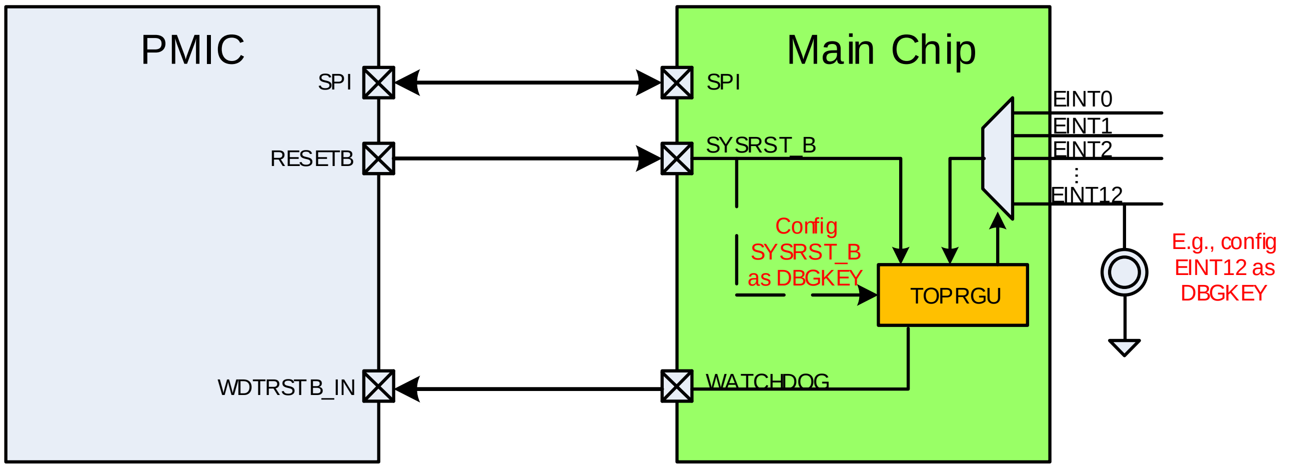
AP JTAG

Design Notice: RAMDUMP - External Key Support (1/2)

- Keyword
  - TOPRGU: Top Reset Generation Unit
- Description
  - The original RAMRUMP is triggered only after system hang and reboot through TOPRGU.
  - This new feature supports RAMRUMP triggered by external key (IO).
  - External ramdump debug key feature must use as a test point or reset button, not a real user key; otherwise it will have mis-trigger problem.

Design Notice: RAMDUMP - External Key Support (2/2)

- [Option A: Recommended] Use one of existing EINT[0:12] pins as debug key
  - The function is default **DISABLED** and can be **reset by TOPRGU.**
  - Input polarity is active **LOW.**
  - EINT DBGKEY has debounce logic.
  - EINT source selection is controlled by TOPRGU.
- [Option B] Reuse SYSRST_B as debug key (IO)
  - SYSRSTB DBGKEY enable is a **non-reset register.**
  - The function is default **ENABLED.**



GPIO Application Notice

Design Notice: GPIO Selection (1/8)

- Be careful of GPIO with 2.8V power domain for 12nm.
- MT6765 GPIO
  - Supports 179 GPIOs belonging to 10 power domains
  - Power domains of GPIO:
    - DVDD18_IORB (1.8V)
    - DVDD18_IOLT (1.8V)
    - DVDD18_IOLM (1.8V)
    - DVDD18_IOBL (1.8V)
    - DVDD18_IORT (1.8V)
    - DVDD18_MSDC0 (1.8V)
    - DVDD18_MSDC1 (1.8V)
    - DVDD28_MSDC1 (1.86V/3.0V)
    - DVDD18_SIM (1.8V)
    - DVDD28_SIM1/DVDD28_SIM2 (1.8V/3.0V)

Design Notice: GPIO Selection (2/8)

- Remove analog GPIO & EINT function
  - AUXIN0 ~4
  - DSI0
  - CSI0 / CSI1 / CSI2
  - WBG IQ

Design Notice: GPIO Selection (3/8)

- Pull-up/Pull-down selection
  - Choose GPIO with suitable PU/PD after reset state for application
    - Example: For "enable pin of audio amplifier", choose GPIO with **PD** after reset state.
    - Example: For "enable pin of external LDO", choose GPIO with **PD** after reset state.

- Power domain of IO supply selection
  - Choose GPIO with suitable power domain of IO supply for application.

- Choose suitable GPIO for peripheral IC
  - Choose GPIOs with matched direction, pull-up/pull-down, data output, GPIO mode after reset state for peripheral IC application.
  - The **enable pin** of acoustic devices or optoelectronic devices (e.g. SPK AMP/Backlight/Charger OCP/OVP) suggest to use **Peripheral_EN[0:5]**

Design Notice: GPIO Selection (4/8)

- **Notice on DCT_Tool usage**

After enabling "InPull En", change the PU/PD value by changing "InPull SelHigh".
(Only valid when GPIO is in input mode)

"InPull En" can enable/disable PU/PD; then GPIO will be the default PU/PD value after reset state.
(Only valid when GPIO is in input mode)

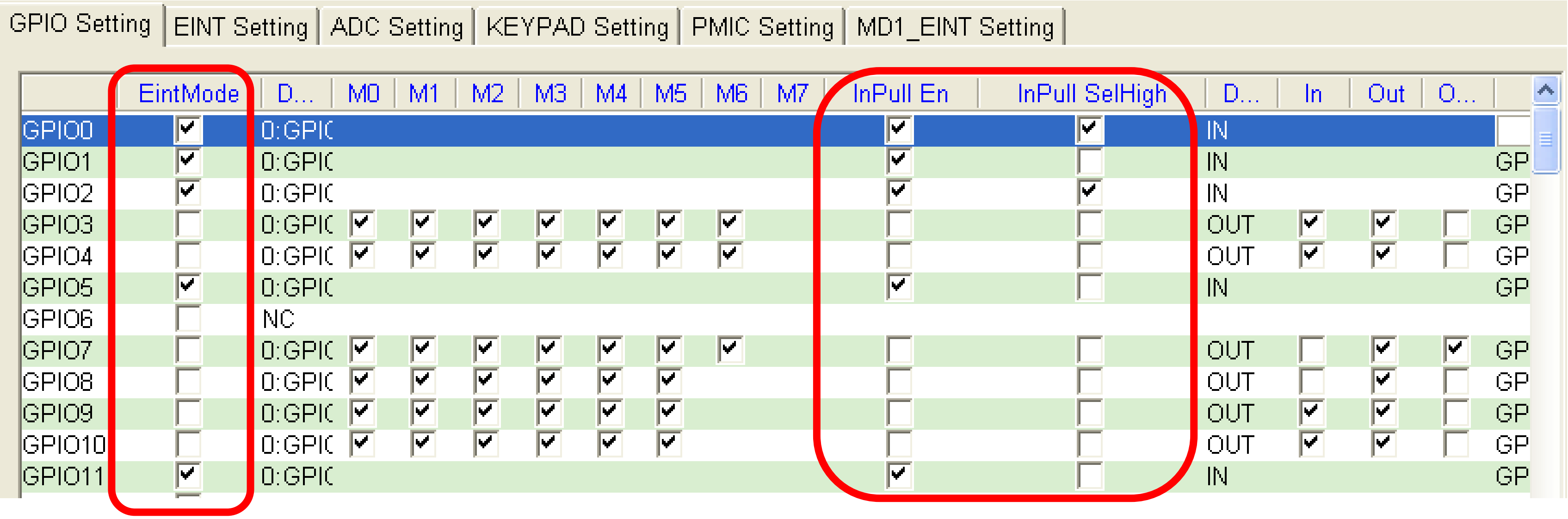
"OutHigh" can change the default output level.
(Only valid when GPIO is in output mode)

GPIO Setting | I2C Setting | CLOCK BUFFER Setting | EINT Setting | ADC Setting | KEYPAD Setting | PMIC Setting | TDSEL/RDSEL | MD1_EINT Setting

	EintMode	Def.Mode	M0	M1	M2	M3	M4	M5	M6	Suspend_State	InPull En	InPull SelHigh	Def.Dir	In	Out	OutHigh
GPIO3	☑	0:GPIO3									☑	☐	IN			
GPIO4	☑	0:GPIO4									☑	☐	IN			
GPIO5	☑	0:GPIO5									☑	☐	IN			
GPIO6	☑	0:GPIO6									☑	☐	IN			
GPIO7	☑	0:GPIO7									☑	☐	IN			
GPIO8	☑	0:GPIO8									☑	☑	IN			
GPIO9	☑	0:GPIO9									☑	☑	IN			
GPIO10	☐	0:GPIO10	☑		☑					INPUT_PD	☐	☐	OUT	☑	☑	☐
GPIO11	☐	0:GPIO11	☑		☑					INPUT_PD	☐	☐	OUT	☑	☑	☐
GPIO12	☑	0:GPIO12								INPUT_PD	☑	☐	IN			
GPIO13	☐	0:GPIO13	☑		☑					INPUT_PD	☐	☐	OUT	☑	☑	☐
GPIO14	☐	0:GPIO14	☑		☑	☐	☐	☐	☐	INPUT_PD	☐	☐	OUT	☑	☑	☐
GPIO15	☐	0:GPIO15	☑		☑	☐	☐	☐	☐	INPUT_PD	☐	☐	OUT	☑	☑	☐
GPIO16		1:IDDIG	☐	☑	☐	☐	☐				☑	☑				☐
GPIO17		1:SIM1_SCLK	☑	☑	☑					INPUT_PD	☐	☐	OUT	☑	☑	☐
GPIO18		1:SIM1_SRST	☑	☑	☑					INPUT_PD	☐	☐	OUT	☑	☑	☐

Design Notice: GPIO Selection (5/8)

- **MT6765 have no dedicated EINT MUX mode.**
  - **GPIO[0:112] can be configured as "External interrupt mode".**
  - **Click EintMode in DCT tool for external interrupt application.**
  - **After EintMode is selected, this pin will be limited for interrupt usage.**
  - **You can set up pull-up or pull-down in "InPullEn" & "InPull SelHigh".**



Design Notice: GPIO Selection (6/8)

- High voltage IO design guide
  - MT6765 (12nm) process IO can sustain 1.8V for general applications.
    - Maximum IO voltage is 1.98V.
  - For application requiring IO voltage over 1.98 volt, 1V8/2V8 IO design is required.
    - Be careful of the schematic design for different applications.
    - DCT tool should be configured properly based on the schematic design.

Improper design or setting will degrade IO reliability.

Design Notice: GPIO Selection (7/8)

- High voltage IO overview

No.	Power domain	PMIC suggested IO power connection	Application	Application description
1	**DVDD28_MSDC1**	VMC (MT6357)	1st T-card, embedded SD	Digital 3.0V power input for MSDC1 (1st T-card, embedded SD)
		VIO18 (MT6357)	GPIO_1V8	1V8 GPIO
		VIO28 (MT6357)	GPIO_2V8	2V8 GPIO
2	**AVDD33_USB**	MT6357's VUSB (3.3V)	USB	USB_FS/HS/OTG2.0

Design Notice: GPIO Selection (8/8)

- MT6765 supports x113 EINTs
  - **GPIO[0:112]** can be configured as “External interrupt mode”
  - Only EINT[0:15] supports HW de-bounce.

EINT Ports	De-bounce	De-bounce time
EINT [0:15]	HW based	0.125/0.25/0.5/1/16/32/64/128/256/512 ms
EINT [16:112]	SW based	1/16/32/64/128/256/512 ms

  - For MEMS sensor/Sensor Hub application, the interrupt pin must be assigned to EINT[0:12]

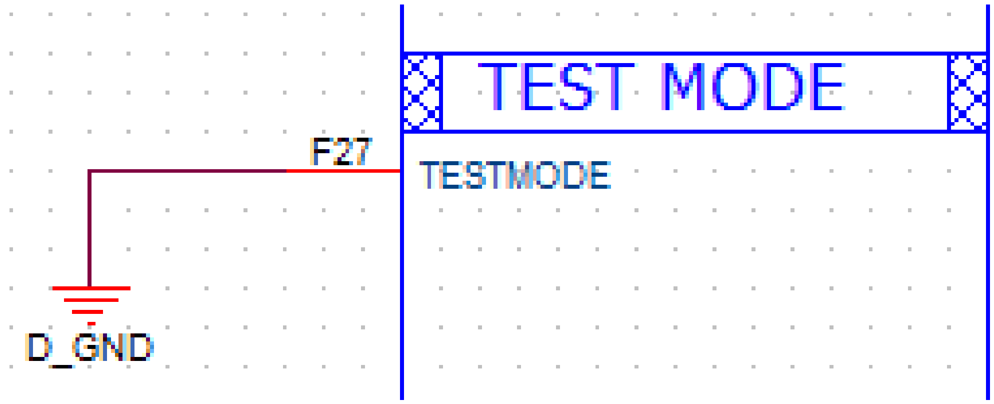
SCH Design Notice

Schematic Notice: Mode Selection

- **Test mode selection**

Chip #	Pin name	Pin out	Normal mode	TEST mode
MT6765	TESTMODE	F27	GND	VIO18 (1.8V)

- For normal usage, configure the pins above to "normal mode".
- TESTMODE is only for debugging. Follow the configuration above.



Schematic Notice: Core Powers (1/3)

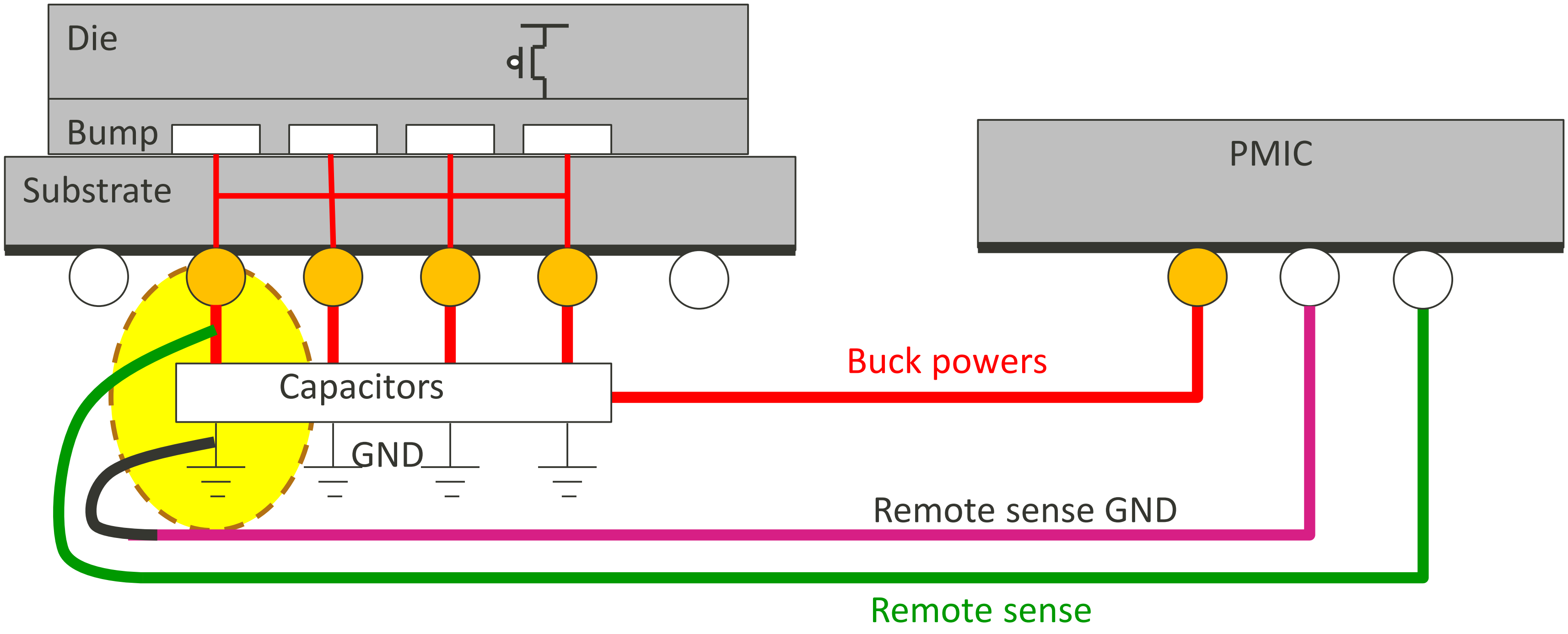
- There are several core power rails which should follow MMD or pass PDN simulation, including VPROC, VCORE, VMODEM, VSRAM_OTHERS, VSRAM_PROC, AVDDQ_EMI and AVDD2_EMI.
- VPROC, VCORE, VMODEM, VSRAM_OTHERS, VSRAM_PROC, AVDDQ_EMI and AVDD2_EMI are powered by dedicated bulk and LDO power source from PMIC (MT6357 & External Buck) respectively.

  * Refer Schematic Notice: DRAM Application

MT6765 core powers	PMIC, MT6357 power source	Buck/LDO	Min. voltage	Max. voltage
VPROC (DVDD_DVFS)	MT6357's VPROC	Buck	0.6	1.12
VCORE (DVDD_TOP, DVDD_MFGSYS, DVDD_MDSYS)	MT6357's VCORE	Buck	0.625	0.8
VMODEM (DVDD_VDD_MODEM)	MT6357's VMODEM	Buck	0.7	0.8
AVDDQ_EMI (AVDDQ_EMI)*	LP3 : PMIC's VDRAM LP4X : External Buck, MT6691O	Buck	-	-
AVDD2_EMI (AVDD2_EMI)*	LP3 : PMIC's VDRAM LP4X : External Buck, MT6691Z	Buck	-	-
VSRAM_PROC (DVDD_MCUSYS_SRAM)	MT6357's VSRAM_PROC	LDO	0.6	1.12
VSRAM_OTHERS (DVDD_TOP_SRAM, DVDD_MFG_SRAM)	MT6357's VSRAM_OTHERS	LDO	0.875	0.875

Schematic Notice: Core Powers (2/3)

- Remote sense design of buck powers (1/2)
  - The remote sense connection of buck powers should be close to MT6765's specific power ball (defined on the next page).



Schematic Notice: Core Powers (3/3)

- Remote sense design of buck powers (2/2)
  - Differential pair of VPROC remote sense should be close to cap on MT6765's DVDD_MCUSYS ball.
  - Differential pair of VCORE remote sense should be close to cap on MT6765's DVDD_MFGSYS ball.
  - Differential pair of VMODEM remote sense should be close to cap on MT6765's DVDD_MODEM ball.

MT6765 core powers	PMIC power source	PMIC power remote sense pin	MT6765 power ball sensed
VPROC (DVDD_DVFS)	MT6357's VPROC	VPROC_FB/ GND_VPROC_FB	Cap on DVDD_DVFS
VCORE (DVDD_TOP, DVDD_MFGSYS, DVDD_MDSYS)	MT6357's VCORE	VCORE_FB/ GND_VCORE_FB	Cap on DVDD_TOP
VMODEM (DVDD_VDD_MODEM)	MT6357's VMODEM	VMODEM_FB/ GND_VMODEM_FB	Cap on DVDD_VDD_MODEM

Schematic Notice: Analog Power

Power	Powered by	De-coupling + power cap.	Function
AVDD12_MD	Ext. VA12*	100nF	Analog power input 1.2V for MD
AVDD18_MD	VIO18	1uF	Analog power input 1.8V for BBTX, BBRX
AVDD12_AP	Ext. VA12*	100nF	Analog power input 1.2V for AP
AVDD18_AP	VIO18	1uF	Analog power input 1.8V for AUXADC, TSENSE
AVDD18_CPU	VIO18	1uF	Analog Power input 1.8V for PTP3 analog modules
AVDD18_DDR	VIO18	1uF + 100nF	Analog power input 1.8V for PLL
AVDD12_PLLGP	Ext. VA12*	100nF	Analog power input 1.2V for PLL
AVDD18_PLLGP	VIO18	100nF	Analog power input 1.8V for PLL
AVDD12_CSI	Ext. VA12*	1uF	Analog power input 1.2V for MIPI CSI
AVDD12_DSI	Ext. VA12*	1uF	Analog power input 1.2V for MIPI DSI
AVDD04_DSI	VCORE	1uF	Analog power input for MIPI DSI
AVDD12_USB	Ext. VA12*	100nF	Analog power input 1.2V for USB
AVDD18_USB	VA18	1uF	Analog power input 1.8V for USB
AVDD33_USB	VUSB	1uF	Analog power input 3.3V for USB
AVDD12_WBG	Ext. VA12*	100nF	Analog power input 1.2V for WBG
AVDD18_WBG	VIO18	100nF	Digital power input 1.8V for WBG

* Refer to External Power Requirement Notice

Schematic Notice: General Power

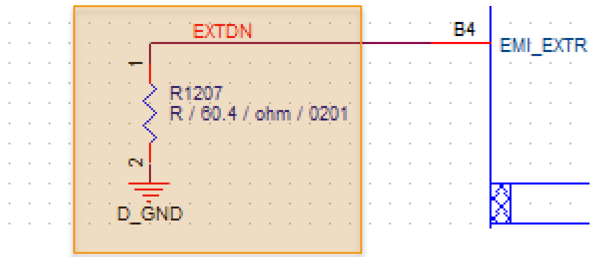
- High speed IO bypass cap. should be of high priority (close to BB).
  - High speed IO bypass cap. should be put close to MT6765.

Power domain	Power by	IO characteristic	Bypass cap.	Function
DVDD18_IOLT DVDD18_IOLM DVDD18_IOBL DVDD18_IOBR DVDD18_IORB DVDD18_IORT	VIO18 (MT6357)	Low speed	100 nF *N (Ref. SCH)	Digital 1.8V power input for IO
DVDD18_MSDC0	VIO18 (MT6357)	**High speed**	100 nF	Digital 1.8V power input for MSDC0
DVDD28_MSDC1	VMC (MT6357)	**High speed**	1uF	Digital 1.86V/3.0V power input for MSDC1
DVDD28_SIM1	VSIM1 (MT6357)	Low speed	100 nF	Digital 1.8V/3.0V power input for SIM1
DVDD28_SIM2	VSIM2 (MT6357)	Low speed	100 nF	Digital 1.8V/3.0V power input for SIM2
DVDD18_SIM	VIO18 (MT6357)	Low speed	100 nF	Digital 1.8V power input for IO Cell
DVDD18_MSDC1	VIO18 (MT6357)	Low speed	100 nF	Digital 1.8V power input for IO Cell

Schematic Notice: LPDDR4X DRAM Application (1/4)

Impedance calibration resistor

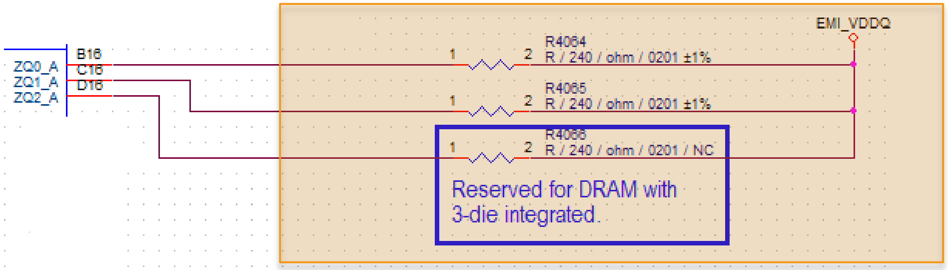
MT6765



MT6765 EMI_EXTR resistor

= 60.4ohm (1%)

DRAM



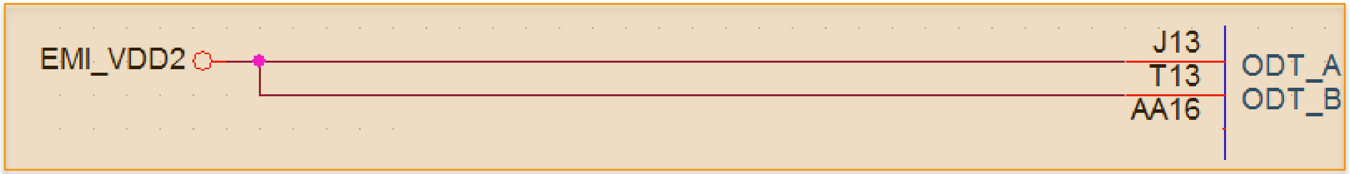
DRAM ZQx resistor

= 240ohm (1%) connect to EMI_VDDQ

Schematic Notice: LPDDR4X DRAM Application (2/4)

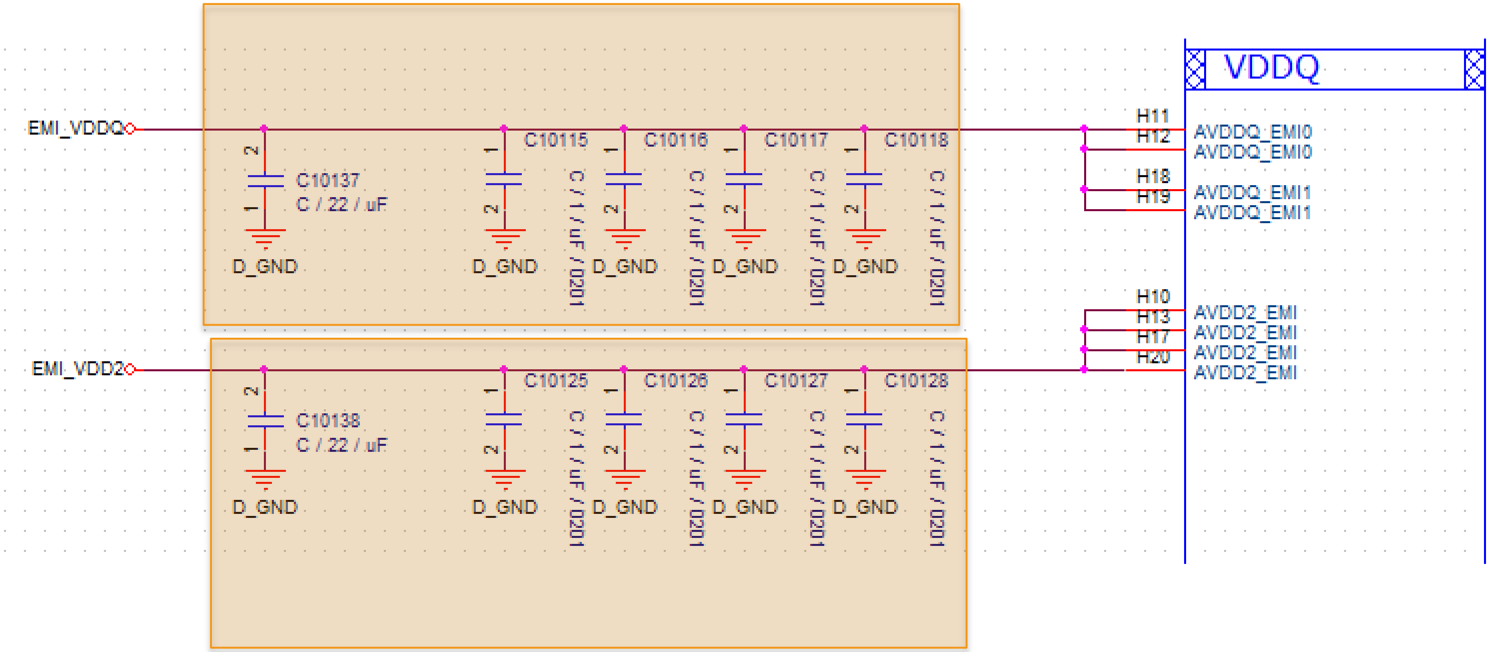
ODT_A/ODT_B

ODT_A/ODT_B pin tied to high(EMI_VDD2)



Schematic Notice: LPDDR4X DRAM Application (3/4)

DRAM Power PDN – AP



AP Side: EMI_VDD2_/EMI_VDDQ 's 1uF capacitor must be close to AP.

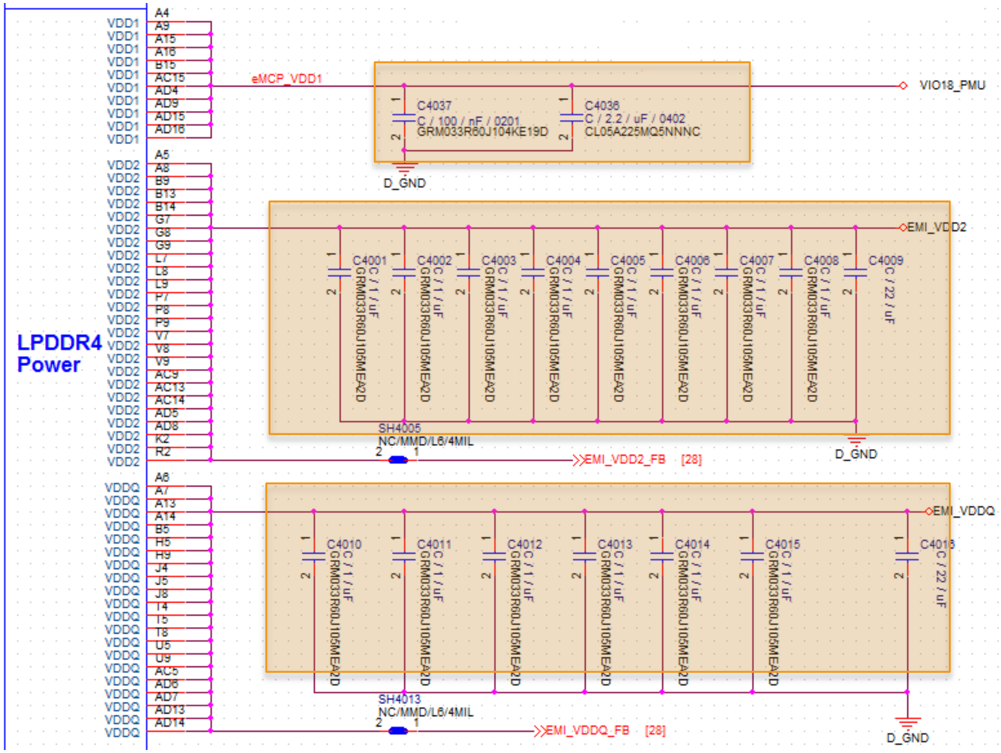
Please refer to MMD.

Schematic Notice: LPDDR4X DRAM Application (4/4)

DRAM Power PDN – DRAM Device

DRAM Side: eMCP_VDD1/EMI_VDD2/EMI_VDDQ 's 0.1uF and 1uF capacitor must be close to DRAM's VDD1/VDD2/VDDQ pins.

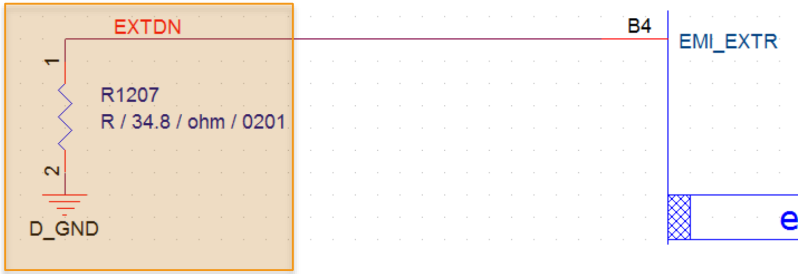
Please refer to MMD.



Schematic Notice: LPDDR3 DRAM Application (1/3)

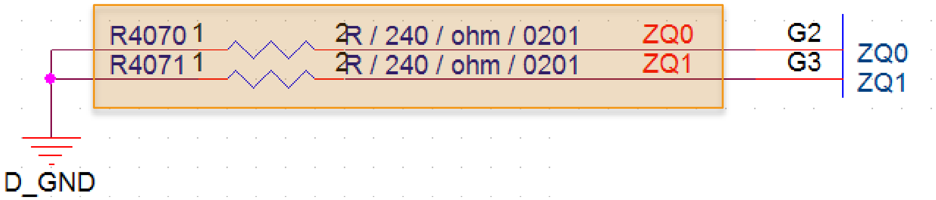
Impedance calibration resistor

MT6765



MT6765 EMI_EXTR resistor
= 34.8ohm (1%)

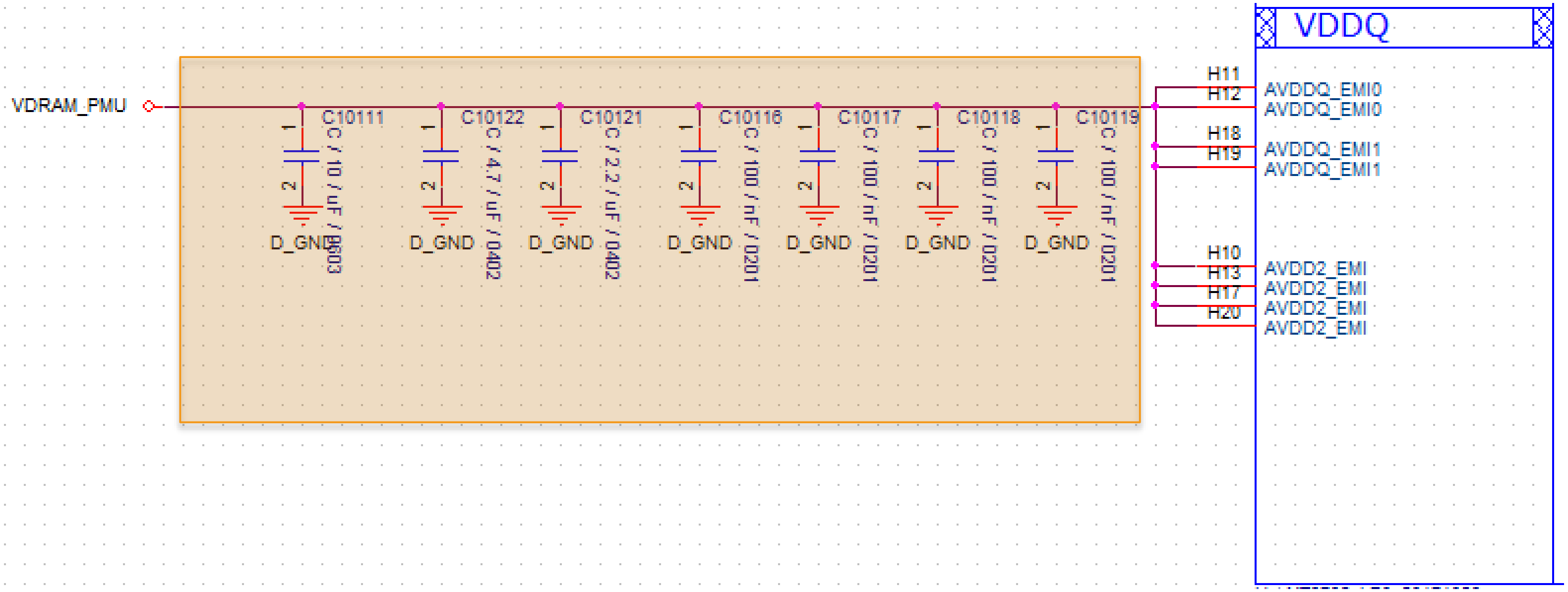
DRAM



DRAM ZQx resistor
= 240ohm (1%) connect to ground

Schematic Notice: LPDDR3 DRAM Application (2/3)

DRAM Power PDN – AP



AP Side: VDRAM_PMU's 100nF capacitor must be close to AP.

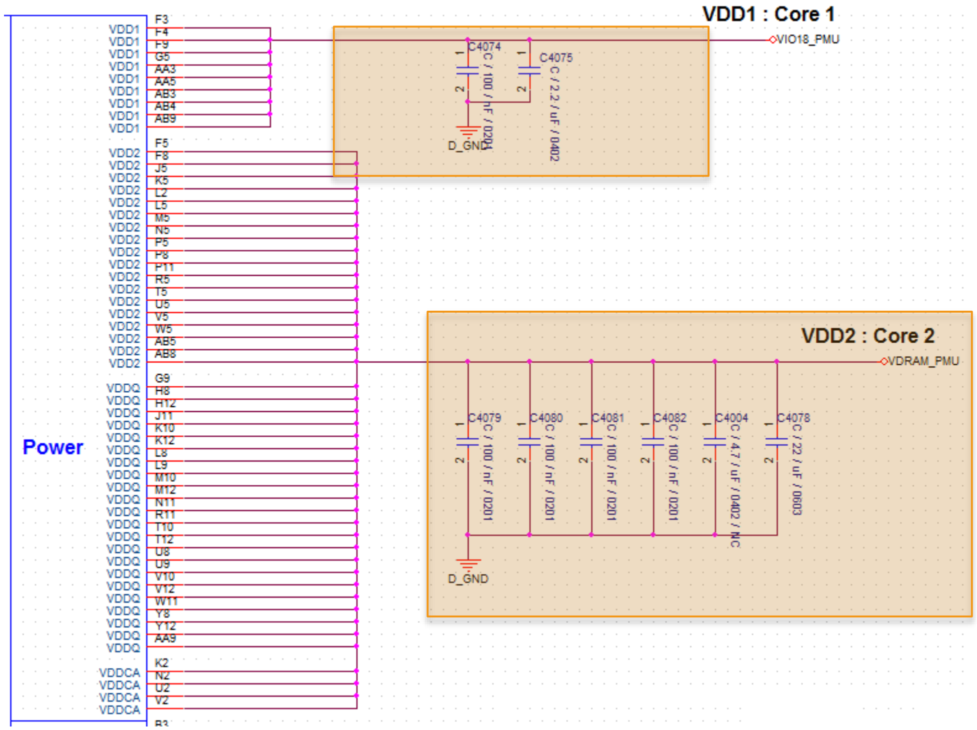
Please refer to MMD.

Schematic Notice: LPDDR3 DRAM Application (3/3)

DRAM Power PDN – DRAM Device

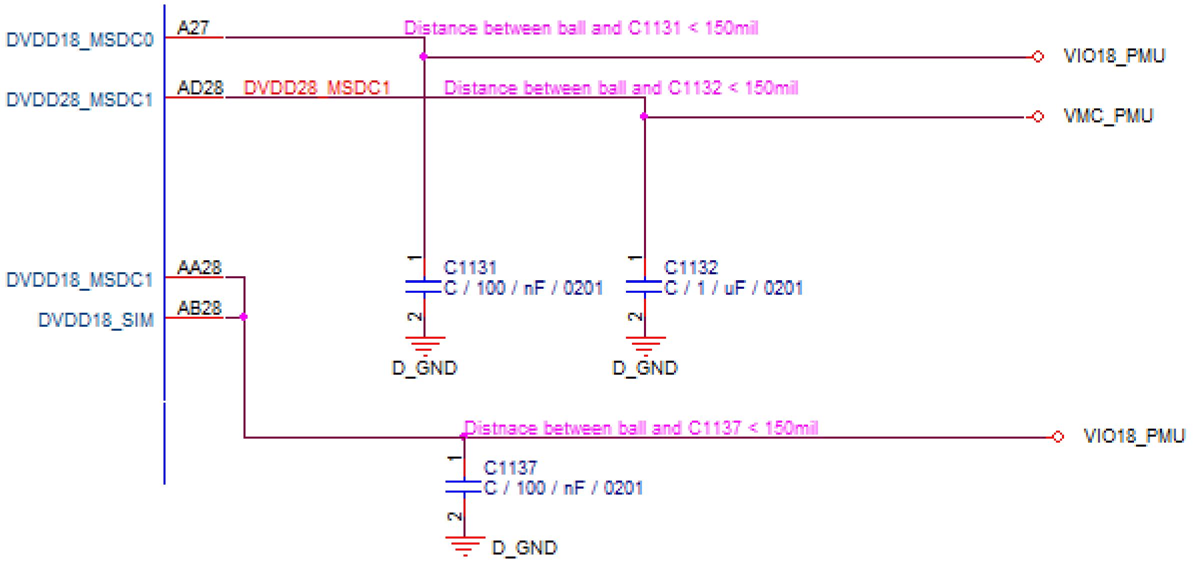
DRAM Side: eMCP_VDD1/VDRAM_PMU's 100nF capacitor must be close to DRAM's VDD1/VDD2/VDDQ pins.

Please refer to MMD.



Schematic Notice: MSDC I/O Pad Power

- **The trace length limit is 150mil.(Must)**
  - **The C1131 must close to Ball: DVDD18_MSDC0**
  - **The C1132 must close to Ball: DVDD28_MSDC1**
  - **The C1137 must close to Ball: DVDD18_MSDC1**



Schematic Notice: eFUSE (1/2)

- **eFUSE programming**

Chip #	Pin name	Pin out	Normal mode	Program mode
MT6765	DVDD_VQPS	AD18	GND	VEFUSE (**Max 1.89V**)

- For normal usage, please configure above pins to “Normal mode”.
- eFuse programming has high-voltage stress time constraint, the maximum accumulative time of eFuse programming when “DVDD_VQPS” =**1.8V+/-5%** should be less than **0.2** sec. (PMIC general LDO VEFUSE)

- **EFUSE programming specification**
  - **Typical 1.8V+/-5%**
  - **Program time : 5us (+/-5%)**
  - **Current consumption : ~200mA**
  - **Vout ramp up time: 30us<t @ Vout =0V to VeFUSE**

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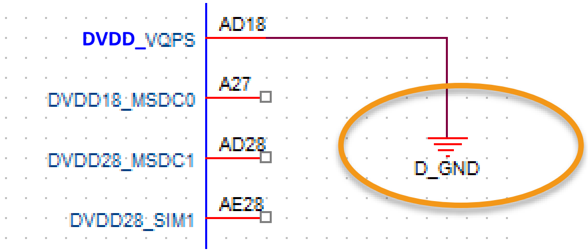
Schematic Notice: eFUSE (2/2)

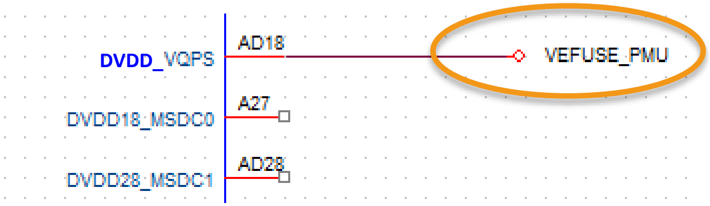
- In no burning eFUSE case, tie pin VQPS to GND

SoC MT6765

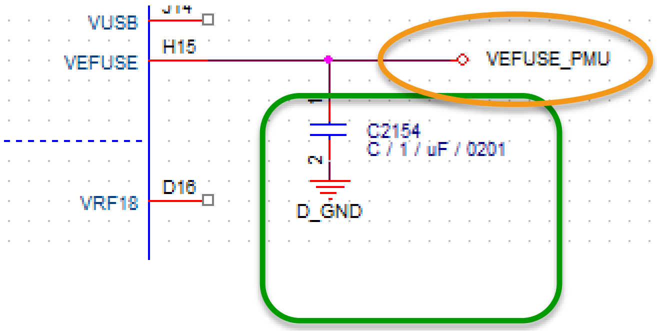


- If burning eFUSE case is needed, pin DVDD_VQPS should be connected to VEFUSE_PMU →Bypass cap should be 1uF

SoC MT6765

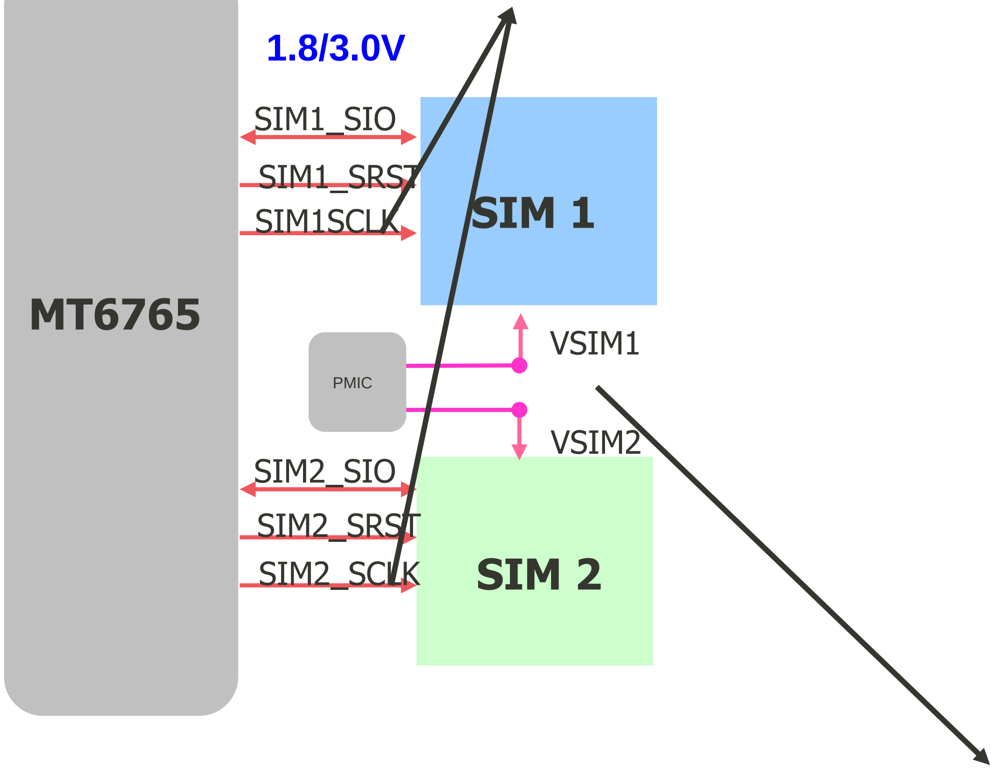


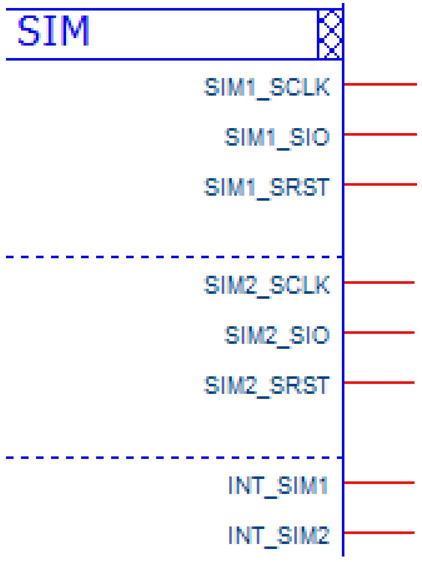
PMIC MT6357



Schematic Notice: Dual SIM

"SCLK" should be shielded by GND"





Reserve 1uF capacitor on the power rails of VSIM, and this capacitor should be placed close to SIM connector.

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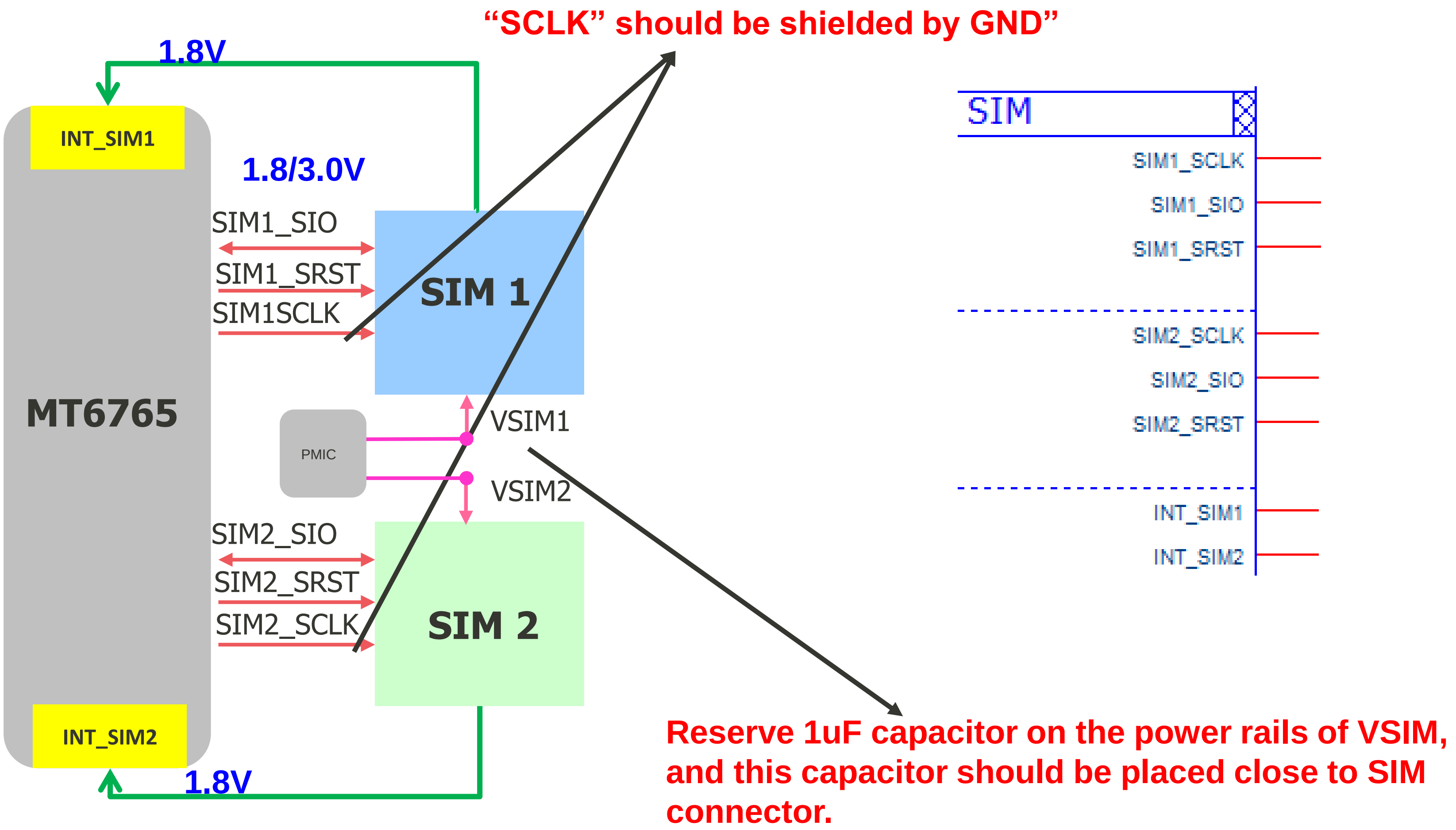
Schematic Notice: SIM Hot Plug (1/2)

- MT6765 support dual SIM Hot Plug application



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Schematic Notice: SIM Hot Plug (2/2)

- MT6765 INT selection for SIM hot plug:

  - For SIM1 hot plug, select ball with pin mux.

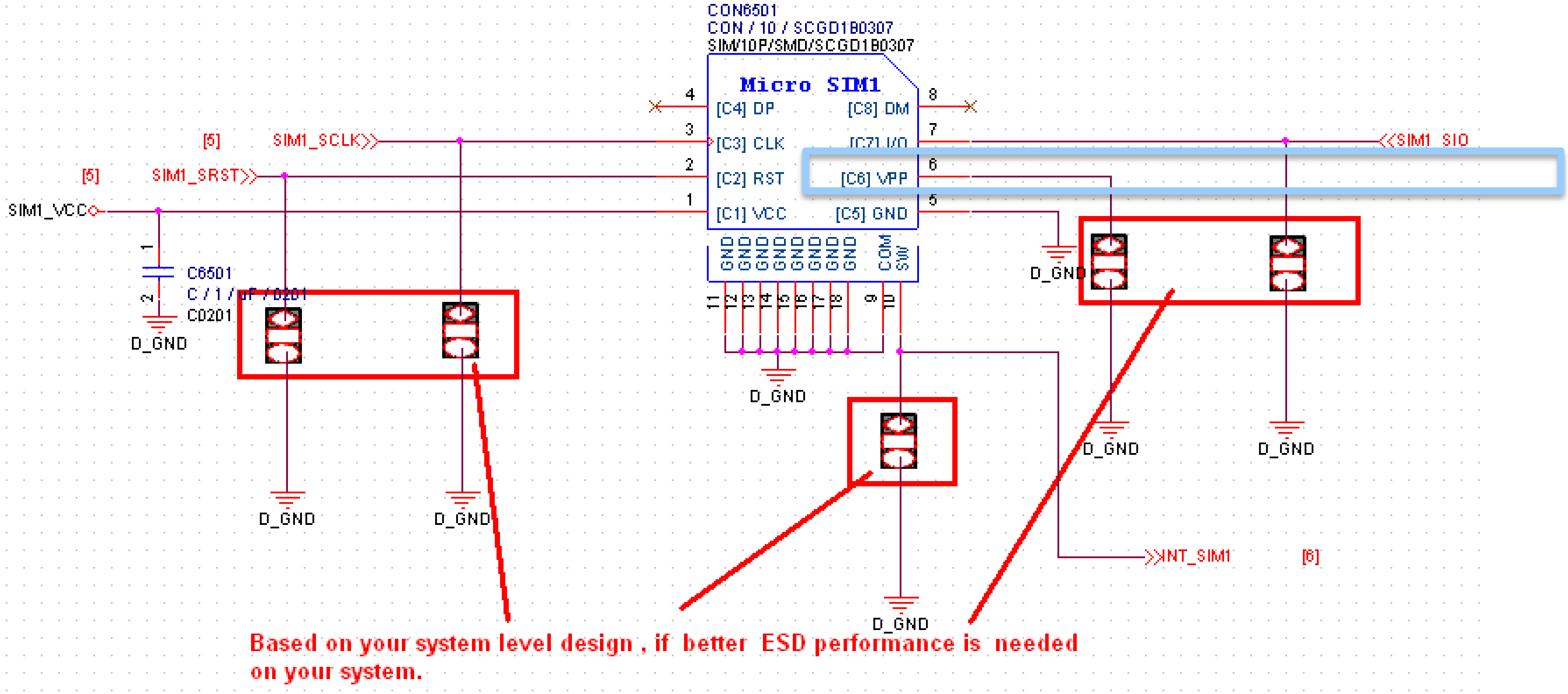
  I0:MD_INT1_C2K_UIM0_HOT_PLUG, e.g. INT_SIM1

  - For SIM2 hot plug, select ball with pin mux.

  I0:MD_INT2_C2K_UIM1_HOT_PLUG, e.g. INT_SIM2

Schematic Notice – Without NFC Application

If your project doesn't have NFC function, VPP[C6] should be NC.(Do NOT connect to VCC[C1])



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For more information about SIM generic design notice, please refer to DMS

(..\HW (For Customer Release) \ Common Design Notes \ SIM)

LCM Design Note – Overview

- MT6765 MIPI DSI Feature

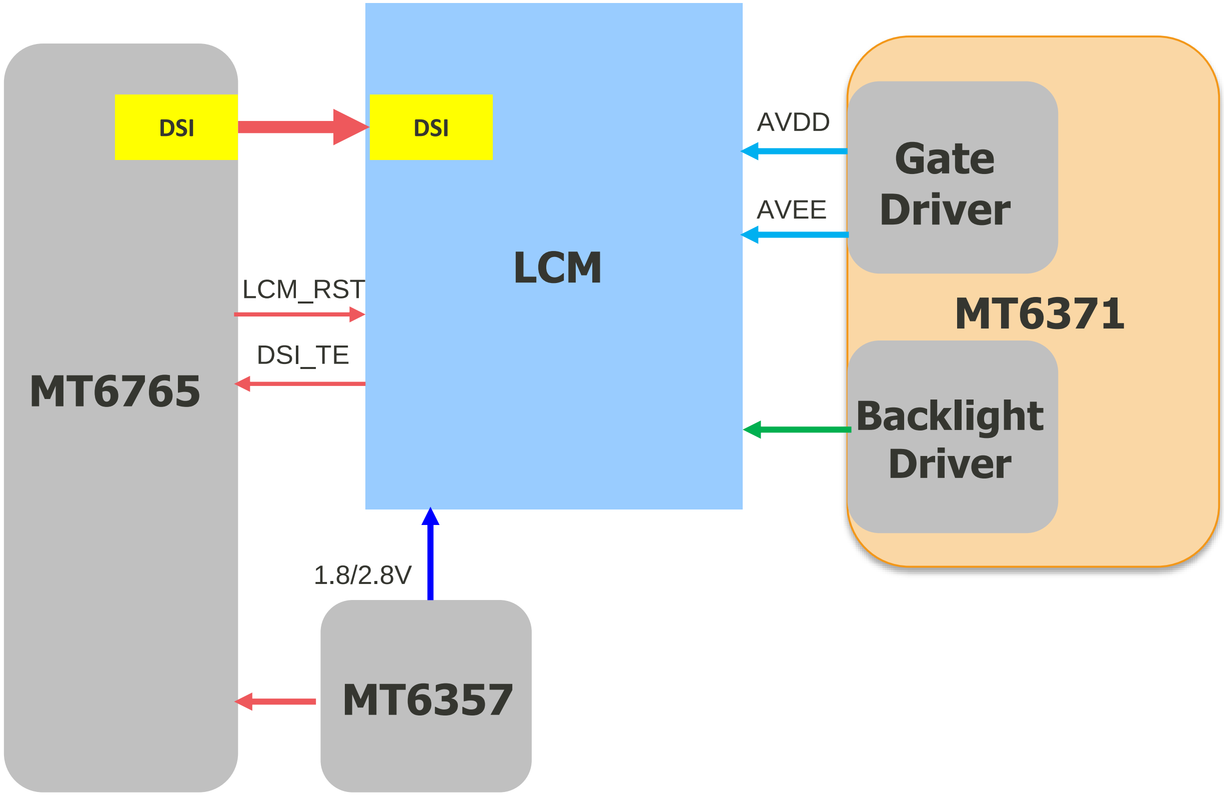
	MT6750T	MT6763	MT6765
Display	**FHD1080 1920x1080**	**FHD1080 1920x1080**	**FHD+1080 2400x1080**
Lane #	4, 1.2Gbps/Lane	4, 1.2Gbps/Lane	4, 1.2Gbps/Lane

- Interface
  - Supports MIPI DSI command/video mode, 4-Lane interface
  - Dedicated HW tearing free control pin for MIPI DSI interface

- IO Power
  - Support 1.8v IO level LCM

LCM Design Note

- LCM side design notice
  - 4 Lane x1 BB and LCM side
  - 4 Lane LCMx1



LCM Design Note

- LCM side design notice
  - Power
    - 2 Power mode
      AVDD(VCI) : connect to 2.8v for LCM analog power
      IOVDD : connect to 1.8v for LCM I/O power
    - 3 Power mode
      IOVDD: connect to 1.8V for LCM I/O power
      AVDD/AVDD: connect to external LCM Gate Drive
  - LCM Data
    - All LCM data pin are reserved at BB side
  - CABC
    - LCM BLC pin or MT6765 DISP_PWM pin connect to external backlight driver
  - System performance
    - EMI filter / Common Choke over LCM control pin & data bus are optional (Trade-off between performance & cost). It could reserve at 1st version SMT.

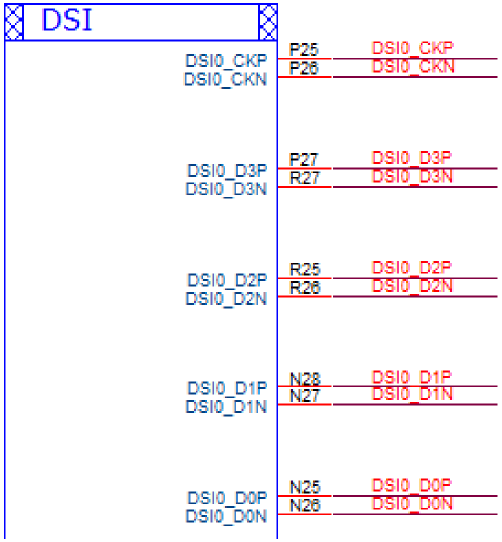
LCM Design Note – MIPI DSI Interface

- BB side design notice
  - MIPI DSI Interface do good to system design simplicity
  - MIPI DSI clk/data are differential pair and trace layout should meet 100ohm differential impedance
    - MIPI_TCP / MIPI_TCN
    - MIPI_TDP0 / MIPI_TDN0
    - MIPI_TDP1 / MIPI TDN1
    - MIPI_TDP2 / MIPI TDN2
    - MIPI_TDP3 / MIPI TDN3

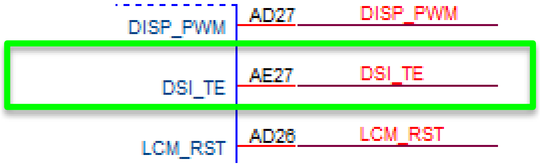
Name	MT6765 Pin
TDN3	DSI0_D3N
TDP3	DSI0_D3P
TDN2	DSI0_D2N
TDP2	DSI0_D2P
TCN	DSI0_CKN
TCP	DSI0_CKP
TDN1	DSI0_D1N
TDP1	DSI0_D1P
TDN0	DSI0_D0N
TDP0	DSI0_D0P

LCM Design Note – MIPI DSI Interface

- MIPI DSI
  - Dedicated MIPI DSI 4-Lane interface.

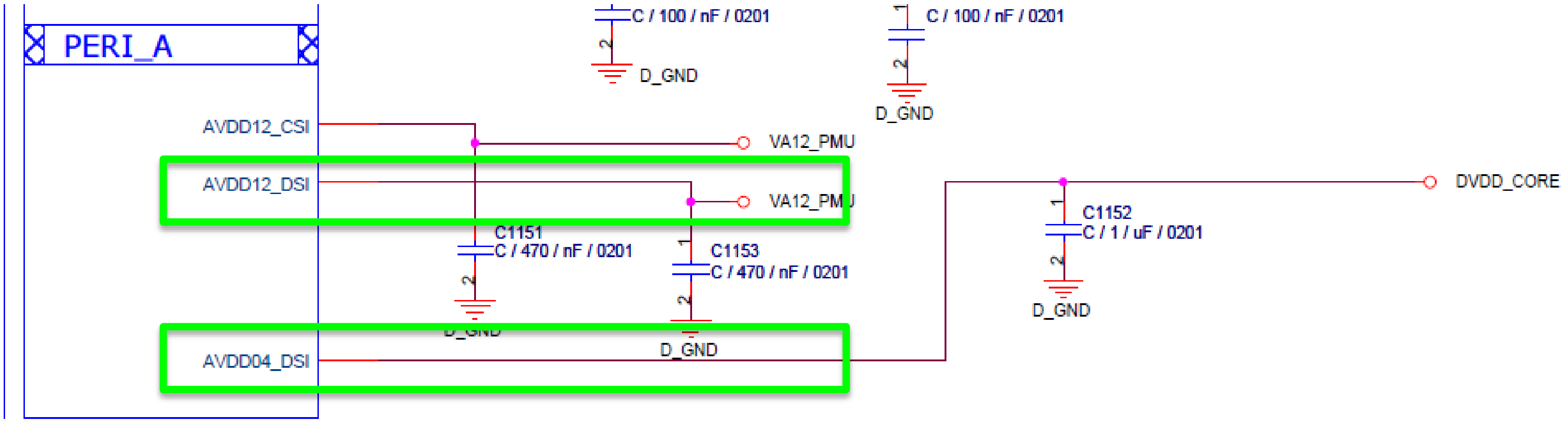


  - DSI_TE MUST be connected to LCM TE Pin.



LCM Design Note – MIPI DSI Interface

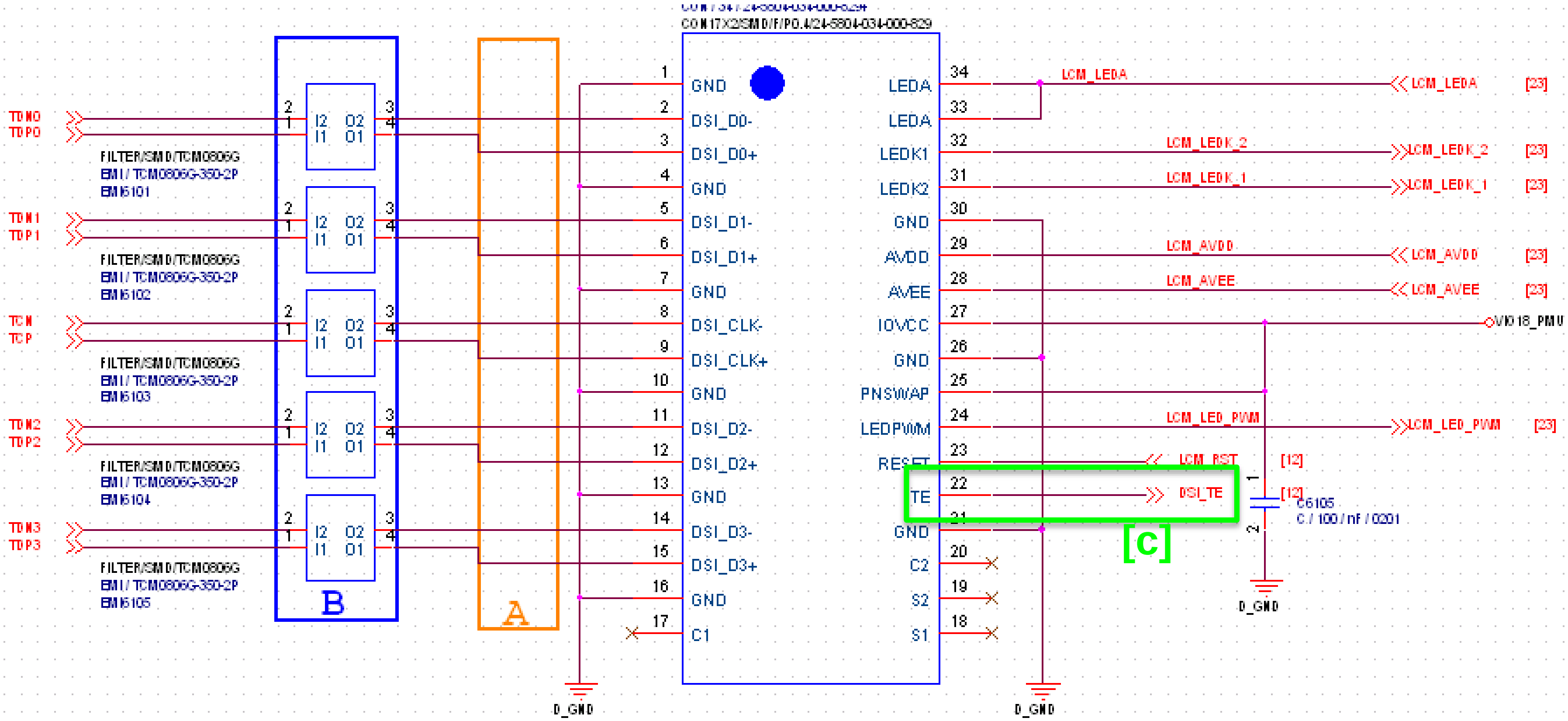
- MIPI Power domain_AVDD04_DSI connected to DVDD_CORE
- MIPI Power domain_AVDD12_DSI connected to VA12_PMU
- By pass cap for MIPI power domain need to close to BB chip



LCM Design Note – Application circuit

– MIPI DSI interface

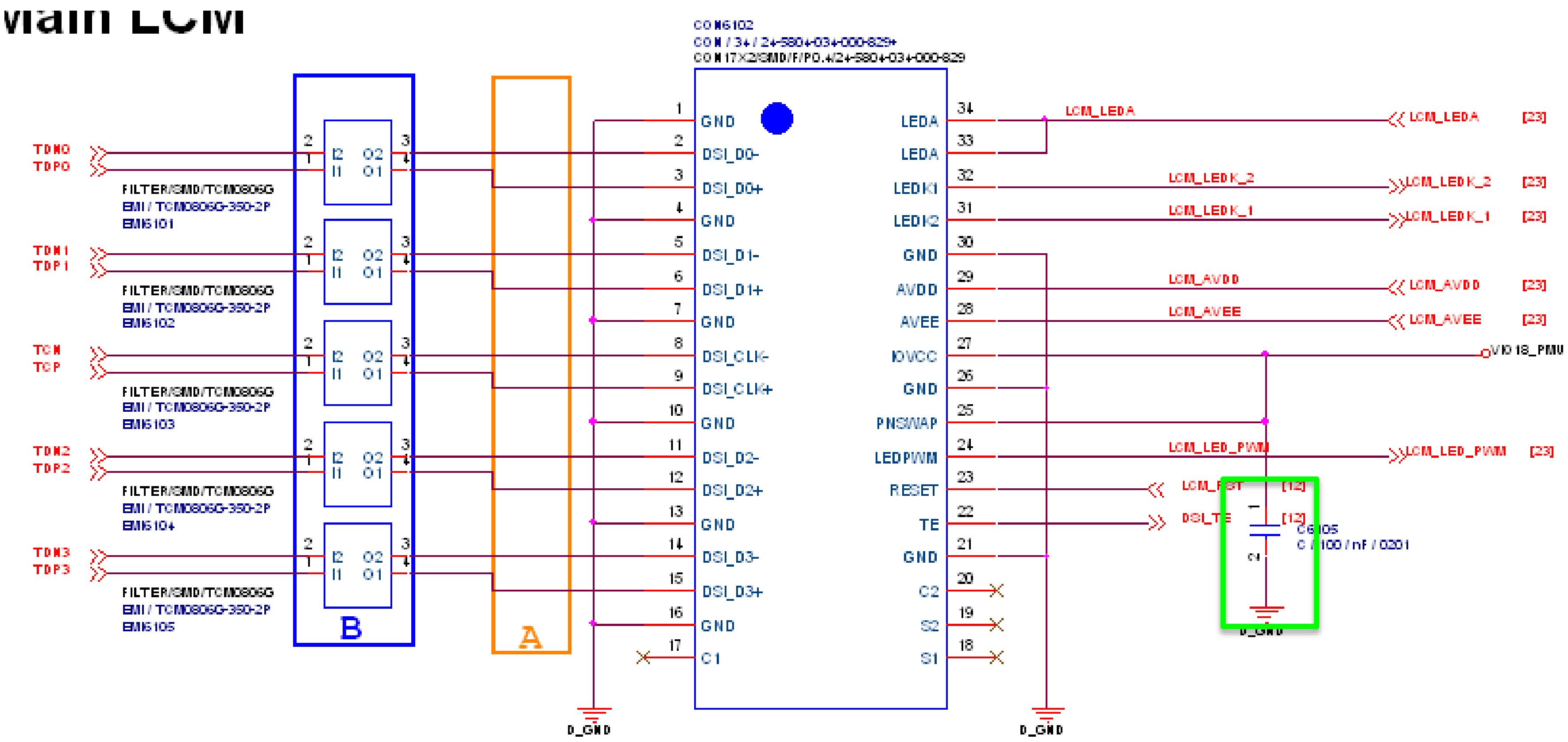
- It is recommended to insert a ground (G) signal between differential pairs to improve inter-lane cross coupling. [A]
- It is recommended to reserve common-mode choke to prevent RF de-sense, the max. cap loading of common-mode choke must be less than 3pF. [B]
- Dedicated HW tearing free control pin for MIPI DSI interface.[C]



LCM Design Note – Application circuit

– Power supply

- IOVCC of LCM module is powered by PMU's VIO18_PMU
- Reserve 100nF capacitor on the power rails of LCM with shunt connection and this capacitor should be placed close to LCM connector.
- AVDD/AVEE and Backlight driver of LCM module is powered by MT6371.



For more information about LCM generic design notice, please refer to DMS

(..\HW (For Customer Release) \ Common Design Notes \ Display)

MT6765 Camera Capabilities

Application scenario	CSI set	Interface /throughput	Sensor resolution @ frame rate per sec.
A	CSI0	CSI 4-lane / 2.8Gbps per lane	25M@30fps
	CSI1	CSI 4-lane / 2.8Gbps per lane	25M@30fps
	CSI2	CSI 4-lane / 2.8Gbps per lane	25M@30fps

Camera MIPI DPHY Interface

CSI #	Pad name	4-lane DPHY mode	2-lane DPHY *2 mode
	CSI0A_L0P	RDP2	RDP0
	CSI0A_L0N	RDN2	RDN0
	CSI0A_L1P	RDP0	RCP
	CSI0A_L1N	RDN0	RCN
	CSI0A_L2P	RCP	RDP1
	CSI0A_L2N	RCN	RDN1
	CSI0B_L0P	RDP1	RDP0-1
	CSI0B_L0N	RDN1	RDN0-1
	CSI0B_L1P	RDP3	RCP-1
	CSI0B_L1N	RDN3	RCN-1
	CSI0B_L2P	X	RDP1-1
CSI-0	CSI0B_L2N	X	RDN1-1
	CSI1A_L0P	RDP2	
	CSI1A_L0N	RDN2	
	CSI1A_L1P	RDP0	
	CSI1A_L1N	RDN0	
	CSI1A_L2P	RCP	
	CSI1A_L2N	RCN	
	CSI1B_L0P	RDP1	
	CSI1B_L0N	RDN1	
	CSI1B_L1P	RDP3	
CSI-1	CSI1B_L1N	RDN3	
	CSI2A_L0P	RDP2	
	CSI2A_L0N	RDN2	
	CSI2A_L1P	RDP0	
	CSI2A_L1N	RDN0	
	CSI2A_L2P	RCP	
	CSI2A_L2N	RCN	
	CSI2B_L0P	RDP1	
	CSI2B_L0N	RDN1	
	CSI2B_L1P	RDP3	
CSI-2	CSI2B_L1N	RDN3	

Note : For MIPI CSI , the unused pins shall be connect to GND

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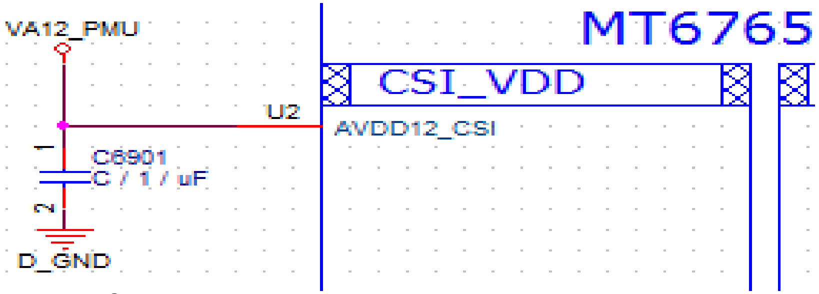
Schematic Notice – Camera (1/6)

- MT6765 Image Sensor Interfaces – MIPI “CSI-2” (1/2)
  - Power
    - **Power name:** AVDD12_CSI
      - Front-facing (Sub-camera) and Rear-facing camera (Main) camera interface is powered by AVDD12_CSI



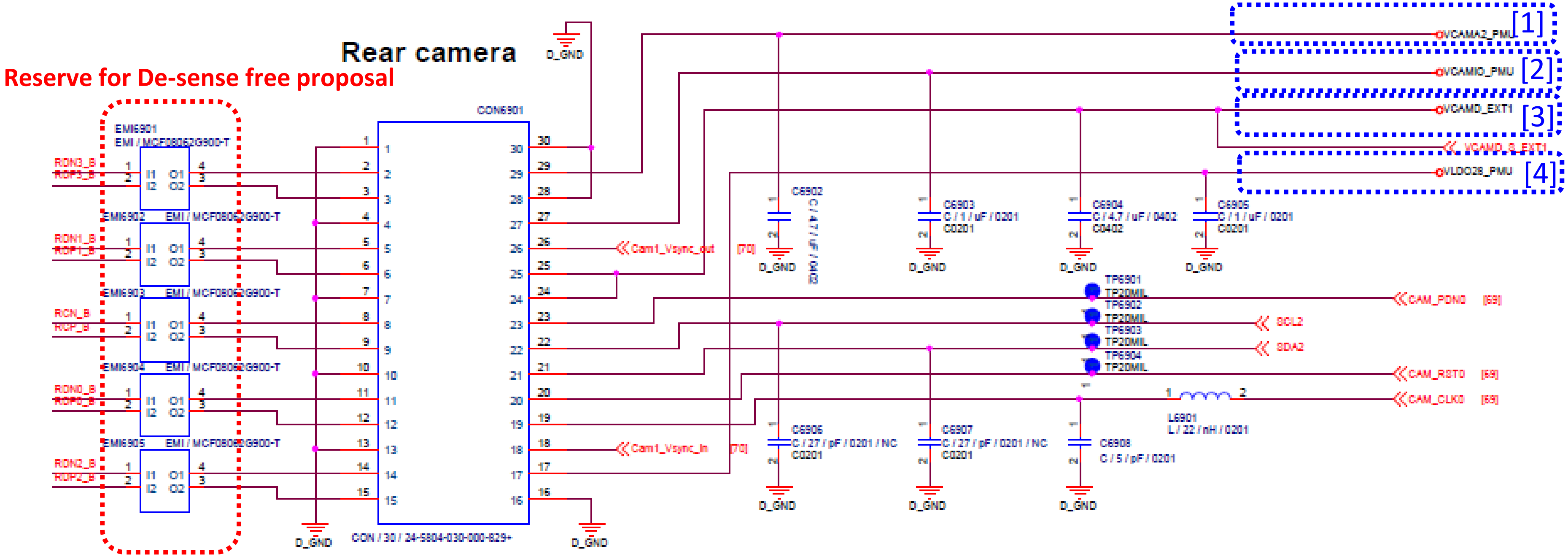
  - MIPI “CSI-2” four-lane interface
    - Differential pair of MIPI CSI, four-lane:
      - RCP (RCP_A) (RCP_B) / RCN (RCN_A) (RCN_B).
      - RDP0 (RDP0_A) (RDP0_B) / RDN0 (RDN0_A) (RDN0_A).
      - RDP1 (RDP1_A) (RDP1_B) / RDN1 (RDN1_A) (RDN1_B).
      - RDP2 (RDP2_A) (RDP2_B) / RDN2 (RDN2_A) (RDN2_B).
      - RDP3 (RDP3_A) (RDP3_B) / RDN3 (RDN2_A) (RDN2_A).

CSI #	Pad name	4-lane DPHY mode	2-lane DPHY *2 mode
	CSI0A_L0P	RDP2	RDP0
	CSI0A_L0N	RDN2	RDN0
	CSI0A_L1P	RDP0	RCP
	CSI0A_L1N	RDN0	RCN
	CSI0A_L2P	RCP	RDP1
	CSI0A_L2N	RCN	RDN1
	CSI0B_L0P	RDP1	RDP0-1
	CSI0B_L0N	RDN1	RDN0-1
	CSI0B_L1P	RDP3	RCP-1
	CSI0B_L1N	RDN3	RCN-1
	CSI0B_L2P	X	RDP1-1
CSI-0	CSI0B_L2N	X	RDN1-1
	CSI1A_L0P	RDP2	
	CSI1A_L0N	RDN2	
	CSI1A_L1P	RDP0	
	CSI1A_L1N	RDN0	
	CSI1A_L2P	RCP	
	CSI1A_L2N	RCN	
	CSI1B_L0P	RDP1	
	CSI1B_L0N	RDN1	
	CSI1B_L1P	RDP3	
CSI-1	CSI1B_L1N	RDN3	
	CSI2A_L0P	RDP2	
	CSI2A_L0N	RDN2	
	CSI2A_L1P	RDP0	
	CSI2A_L1N	RDN0	
	CSI2A_L2P	RCP	
	CSI2A_L2N	RCN	
	CSI2B_L0P	RDP1	

    - The data lane number of MIPI “CSI-2” four-lane can be configured to support 1, 2 or 4 lane.
      - Signals to support 1~n data lane, where n= 4:
        { RCP / RCN } ; { RDP0 / RDN0 } to { RDP(n-1) / RDN(n-1) }
      - Signals to support 1~n data lane, where n= 4:
        { RCP_A / RCN_A } ; { RDP0_A / RDN0_A } to { RDP(n-1)_A / RDN(n-1)_A}
    - The data receiving throughput of MIPI “CSI-2” four-lane interface can up to **2.8Gbps.**
    - For MIPI CSI , the unused pins shall be connect to GND

Schematic Notice – Camera (2/6)

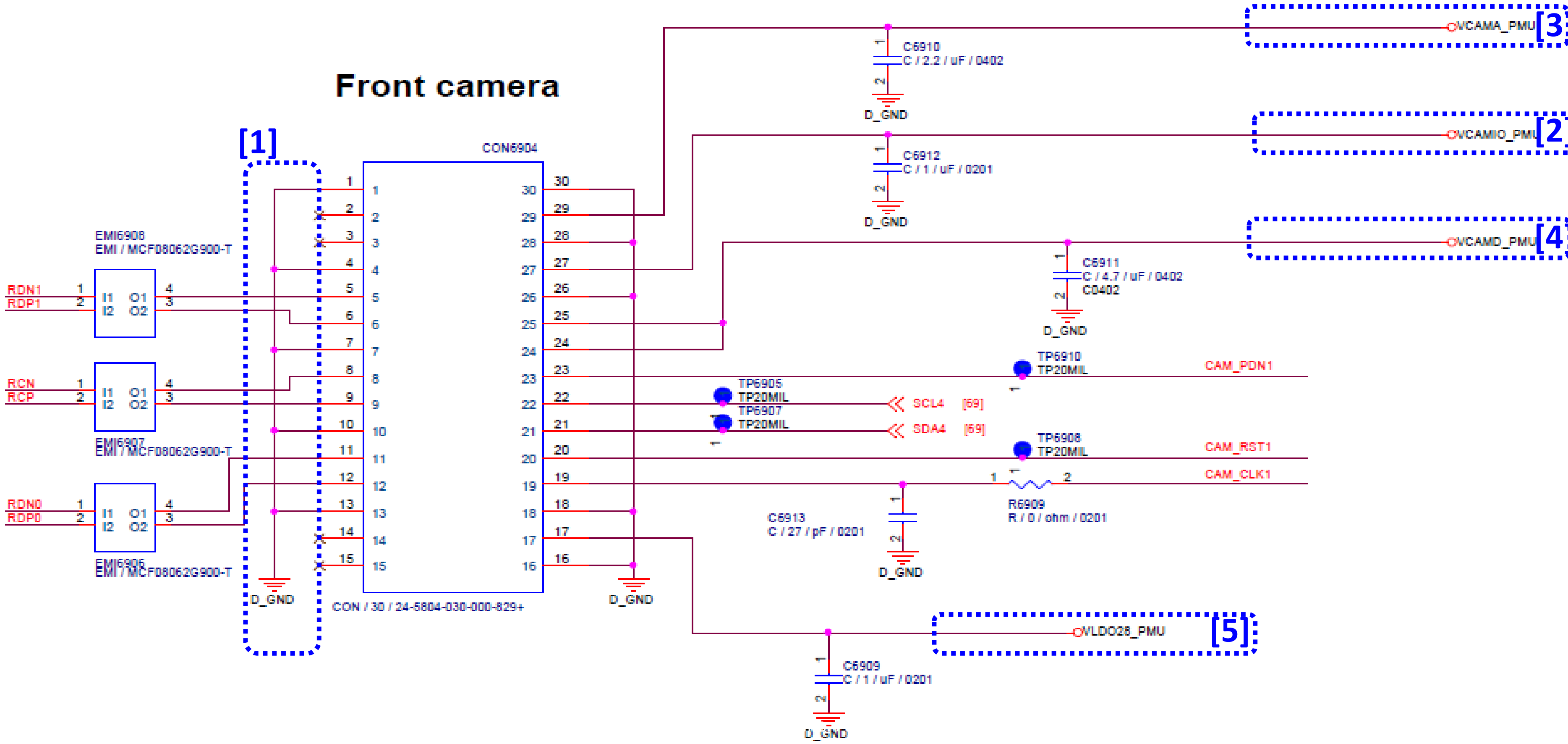
- Application circuit of rear facing camera
  - Power supply (1/2)
    - Analog 2.8V power of camera module is powered by PMU's VCAMA2. [1]
    - I/O 1.8V power of camera module is powered by PMU's VCAMIO. [2]
    - Core power of camera module is powered by External LDO.[3]
    - Auto focus (AF) 3.3V power of camera module is powered by PMU's VLDO28. [4]



NOTE : Please check the voltage / current requirement of your selected camera sensor and compare with the relevant spec of their power source.

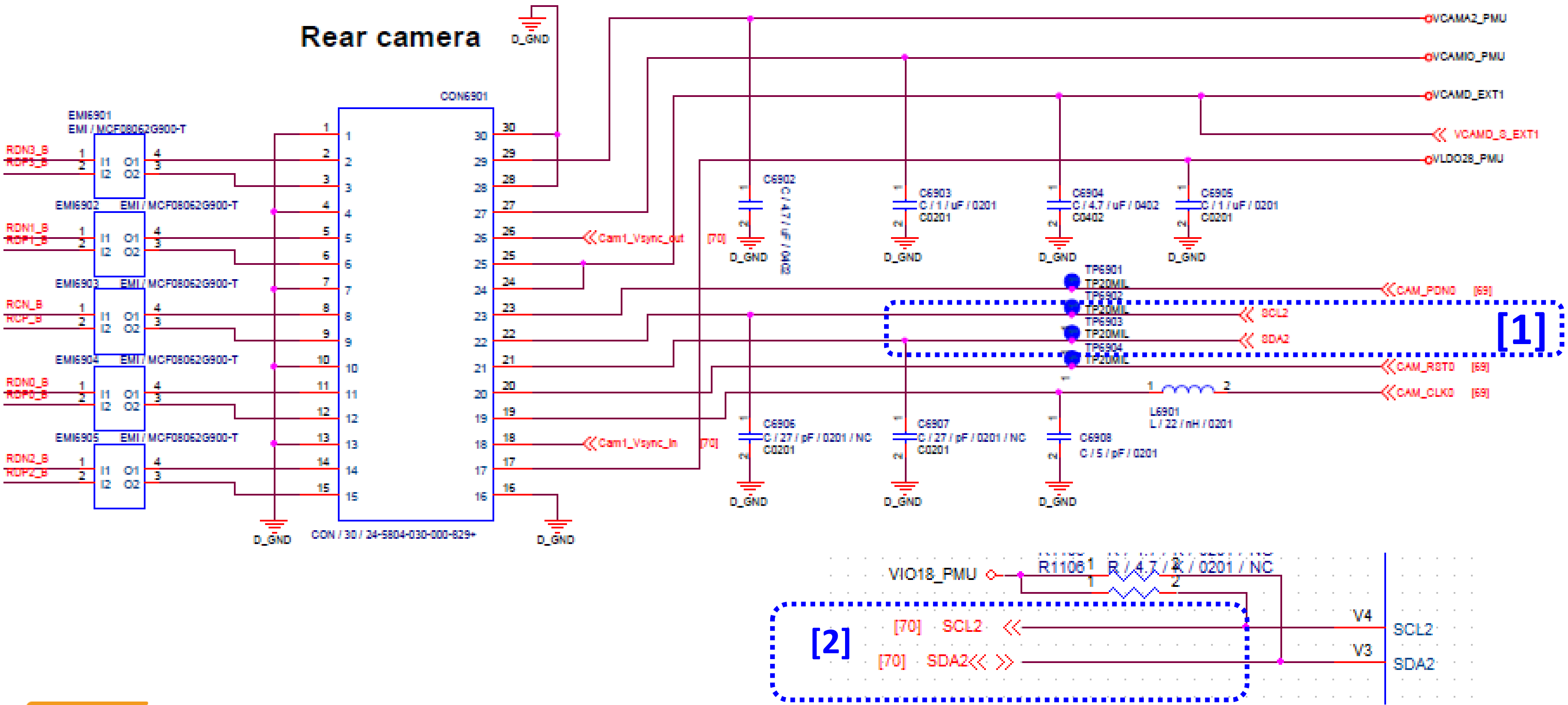
Schematic Notice – Camera (3/6)

- Application circuit of front facing camera
  - MIPI CSI interface
    - It is recommended to insert a ground (G) signal between differential pairs to improve inter-lane cross coupling. [1]
    - I/O 1.8V power of camera module is powered by PMU's VCAMIO. [2]
    - Analog 2.8V power of camera module is powered by PMIC's VCAMA. [3]
    - Core power of camera module is powered by PMIC's VCAMD. [4]
    - Auto focus (AF) 3.3V power of camera module is powered by PMU's VLDO28. [5]



Schematic Notice – Camera (4/6)

- Application circuit of rear facing camera
  - I2C/SCCB control interface
    - The I2C-2 (SCL2 & SDA2) is used to control the Main-camera sensor module. [1]
    - Must have external pull-up resistors for I2C open-drain I/O. In MT6765, I2C are 1Kohm internal pull up in AP side [2]



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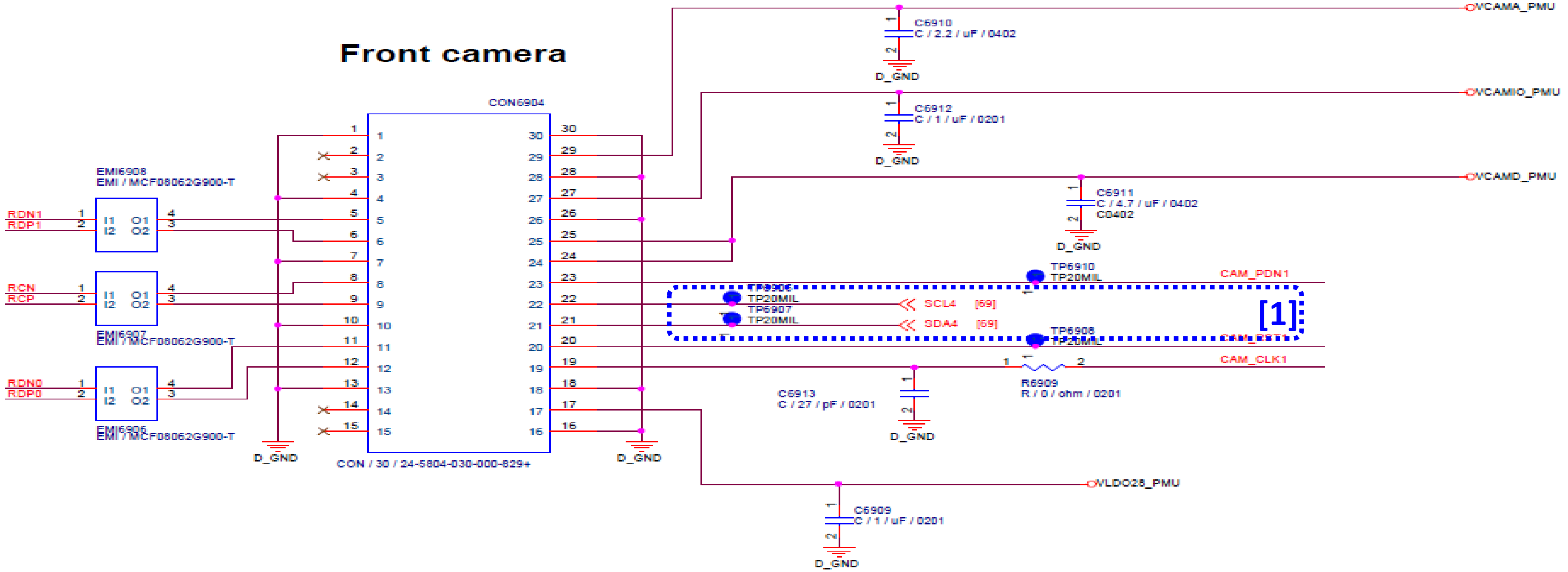
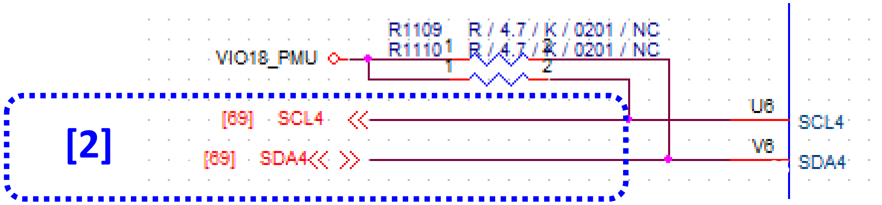
Schematic Notice – Camera (5/6)

- Application circuit of front facing camera
  - I2C/SCCB control interface
    - The I2C-4 (SCL4 & SDA4) is used to control the sub-camera sensor module. [1]
    - Must have external pull-up resistors for I2C open-drain I/O. In MT6765, I2C are 1Kohm internal pull up in AP side [2]

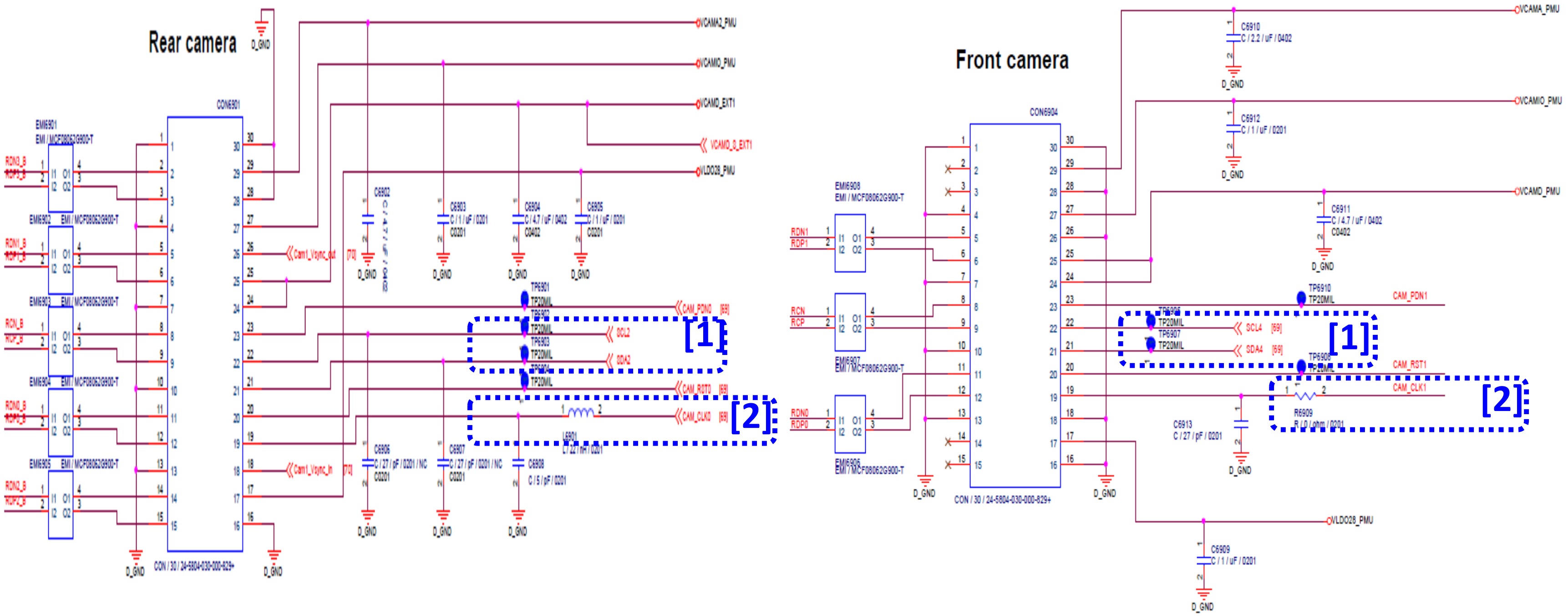




Schematic Notice – Camera (6/6)

- Application circuit of PIP
  - I2C/SCCB control interface
    - The I2C-2 (SCL2 & SDA2) and I2C-4 (SCL4 & SDA4) is used to control the main-camera and the sub-camera, respectively. [1]

      If **support PIP** (picture in picture) function, the I2C **must use** respectively. therefore it will avoid address's conflict.
    - Recommend well GND shielding in **CAM_CLK0 and CAM_CLK1**. [2]



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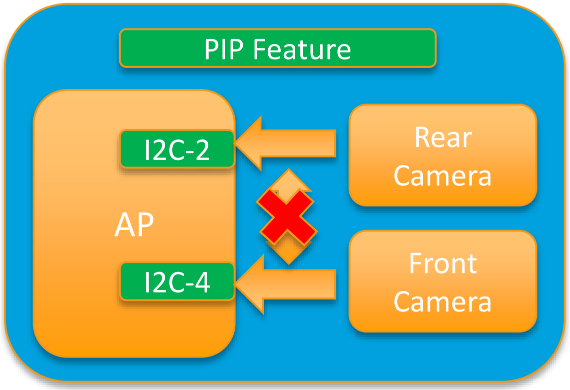
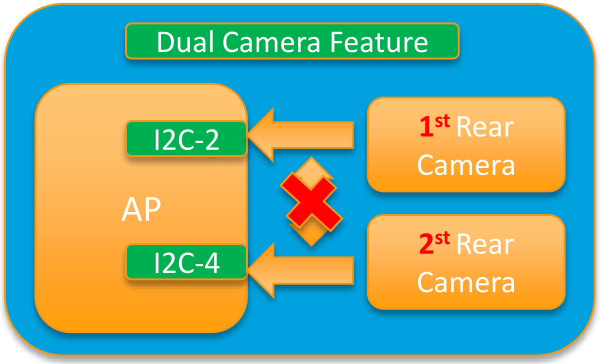
MT6765 PIP Feature Design Note

- **Sensor**
  - No additional limitation on camera sensor selection (shall also on MTK QVL)
- **CMMCLK**
  - Separate CAM_CLK design
    - use **CAM_CLK0** on rear camera, and **CAM_CLK1** on front camera
- **AVDD/DVDD**
  - AVDD of Rear/Front shall be separated
    - Connect Rear/Front to MT6357's VCAMA and External LDO
  - DVDD of Rear/Front shall be separated
    - Connect Rear/Front to MT6357's VCAMD and External LDO
- **I2C**
  - **Rear and Front camera Must use separated I2C** whether AF driver/sensor driver/EEPROM's I2C slave address are the same or not.



MT6765 Dual Camera Feature Design Note

- **Sensor**
  - No additional limitation on camera sensor selection (shall also on MTK QVL)
- **CMMCLK**
  - Separate CAM_CLK design
    - use **CAM_CLK0** on 1st rear camera, and **CAM_CLK2** on 2nd rear camera
- **AVDD/DVDD**
  - AVDD of 1st rear/2nd rear shall be separated
    - Connect 1st rear/2nd rear to MT6357's VCAMA and External LDO
  - DVDD of 1st rear/2nd rear shall be separated
    - Connect 1st rear/2nd rear to MT6357's VCAMD and External LDO
- **I2C**
  - **1st Rear and 2nd Rear Camera Must use separated I2C** whether AF driver/sensor driver/EEPROM's I2C slave address are the same or not

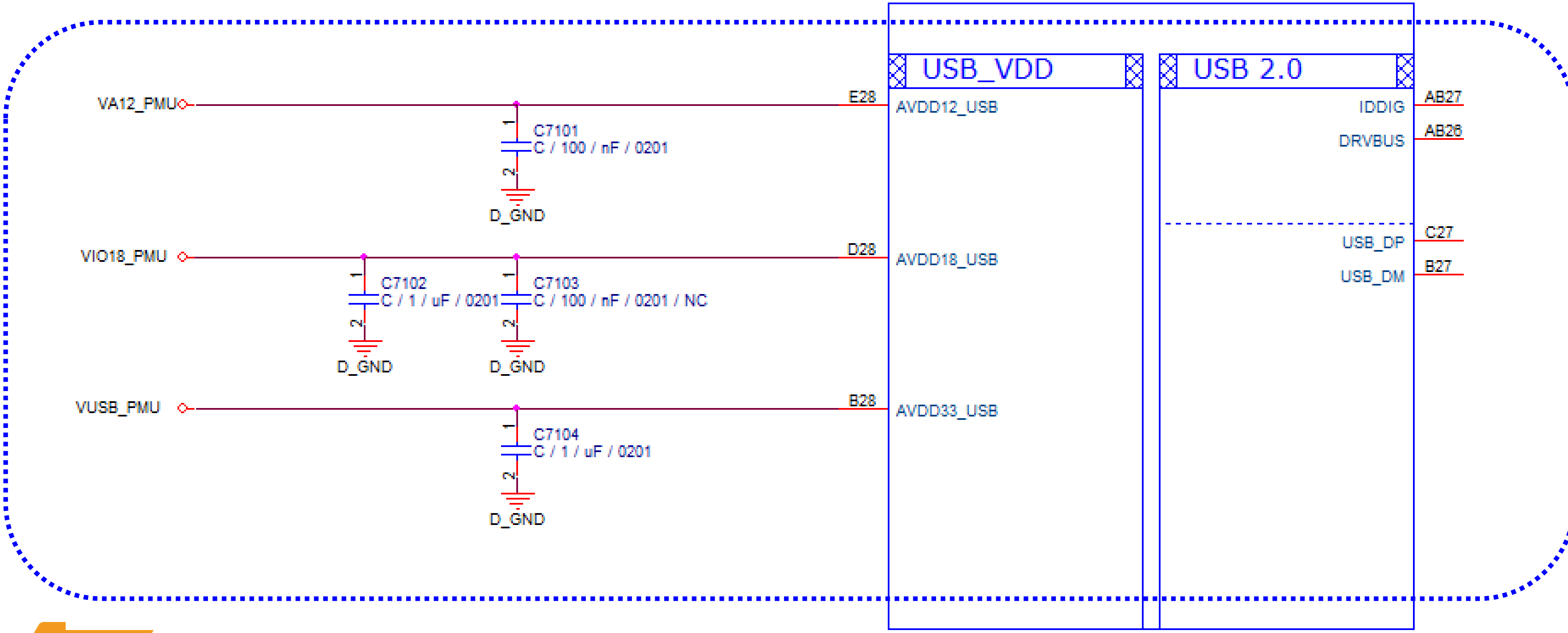


For more information about camera generic design notice, please refer to DMS

(..\HW (For Customer Release) \ Common Design Notes \ Camera)

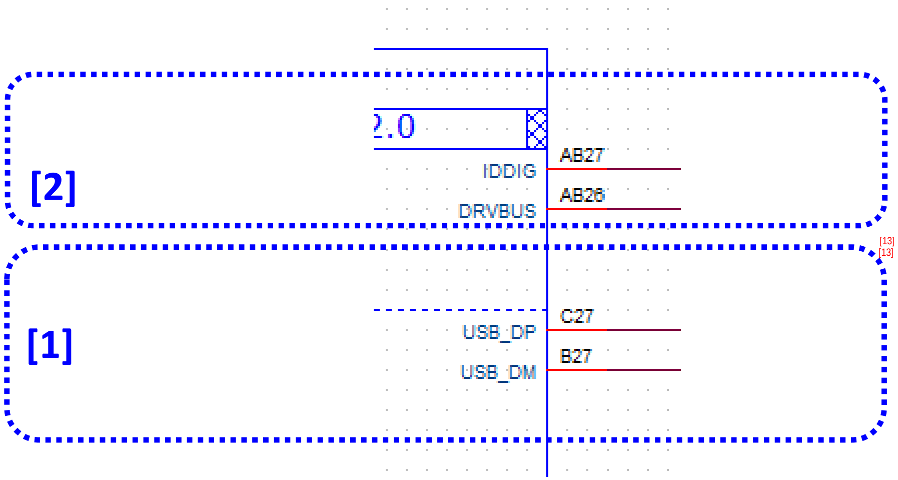
Schematic Notice – USB (1/4)

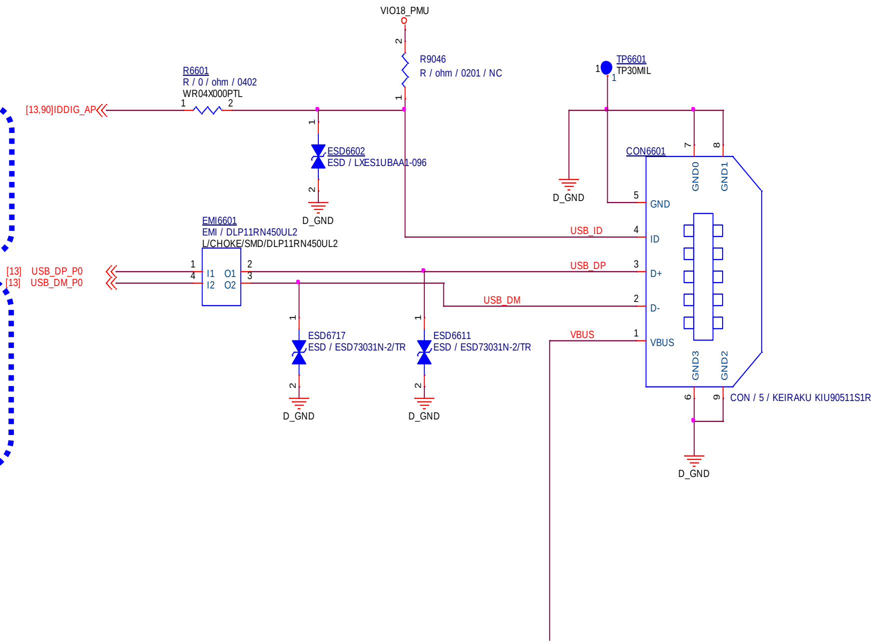
- MT6765 USB Power supply
  - USB Power
    - **USB** (The decouple capacitance should be reserved)
      - **USB HS/FS :** AVDD18_USB / AVDD12_USB / AVDD33_USB_P0
        - AVDD33_USB powered by PMIC VUSB
        - AVDD18_USB powered by PMIC VIO18
        - AVDD12_USB powered by PMIC VA12



Schematic Notice – USB (2/4)

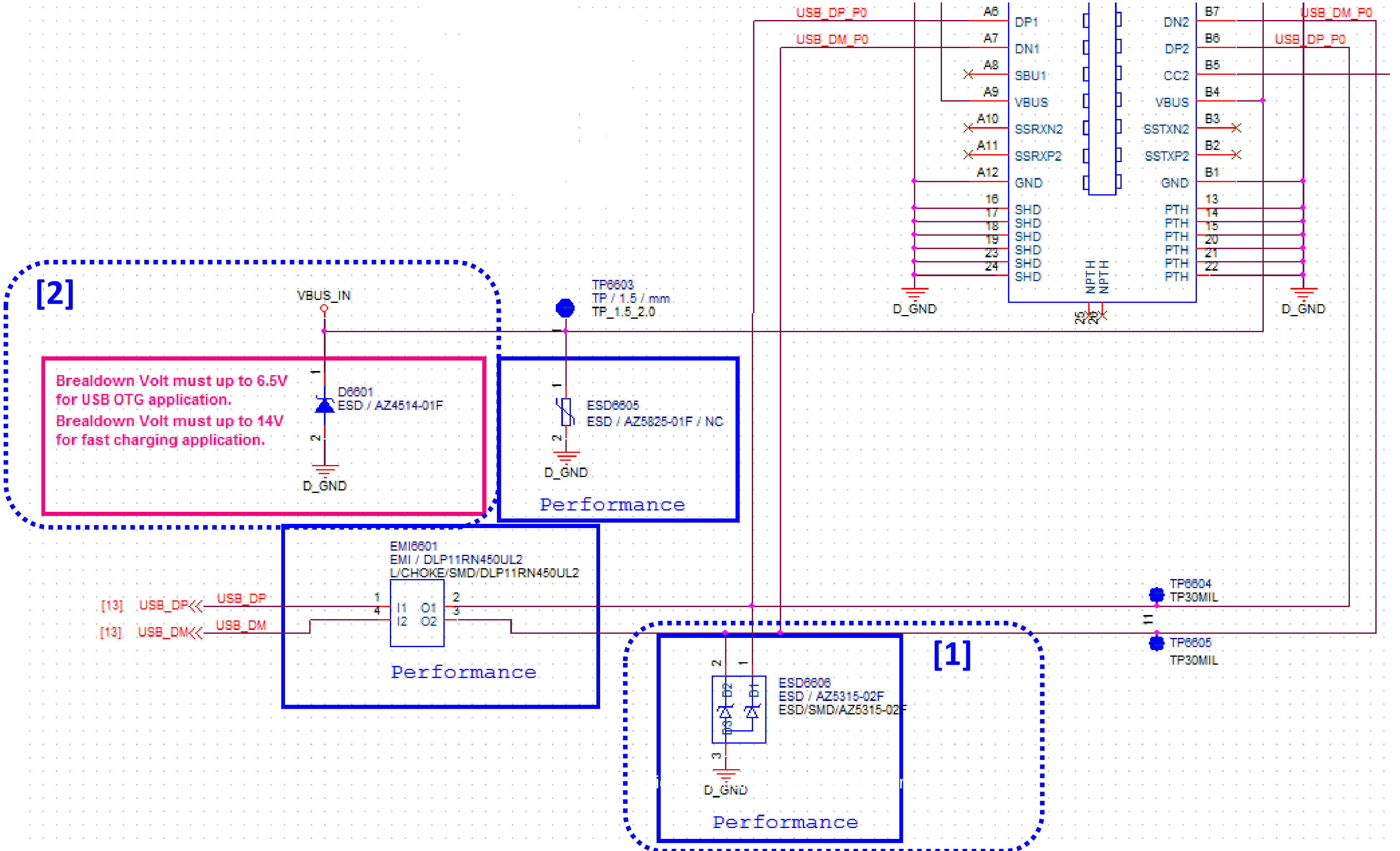
- MT6765 USB schematic (1/3)
  - USB Differential pair: The **90-Ohm** characteristic impedance must be implemented in PCB layout. [1]
    - USB_DM_P0/ USB_DP_P0
  - USB OTG 2.0 support (For Mini USB and Micro USB connector)
    - MT6765 support full OTG function. [2]
    - PMIC will detect VBUS and inform MT6765 to set up USB related signals.
    - IDDIG is detected by GPIO with pull-up 75K ohm resistor. (Recommend Using IDDIG, since the interrupt is always work, even in sleep mode)
    - Beware plug-in a MHL Cable without build-in MHL switch. (It maybe damage the ID pin)





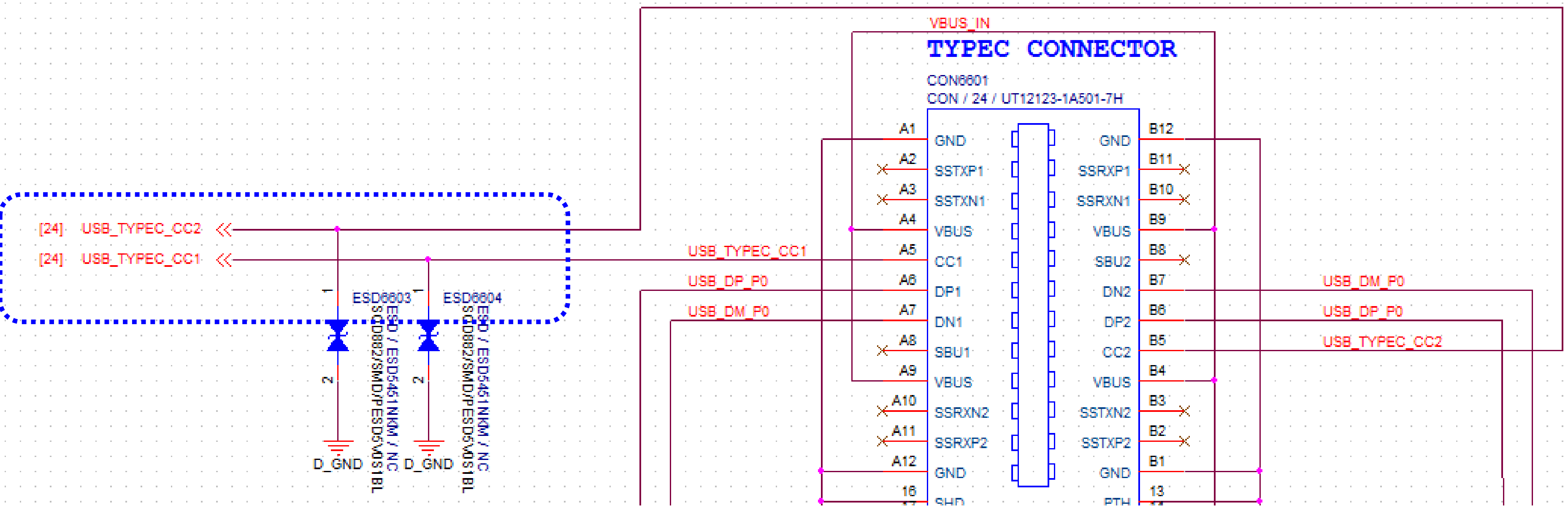
Schematic Notice – USB (3/4)

- MT6765 USB schematic (2/3)
  - USB application circuit on HS/FS receptacle side (For USB type C)
    - In connector side, connect the DP1 to DP2 and DN1 to DN2 directly.
    - The equivalent capacitance loading of ESD protection device should be less than **3pF**. [1]
    - Beware the diode operate voltage for avoid the leakage current. [2]



Schematic Notice – USB (4/4)

- MT6765 USB schematic (3/3)
  - USB application circuit on HS/FS receptacle side (For USB type C)
    - Reserve ESD protection device for USB_TYPEC_CC1 / USB_TYPEC_CC2.

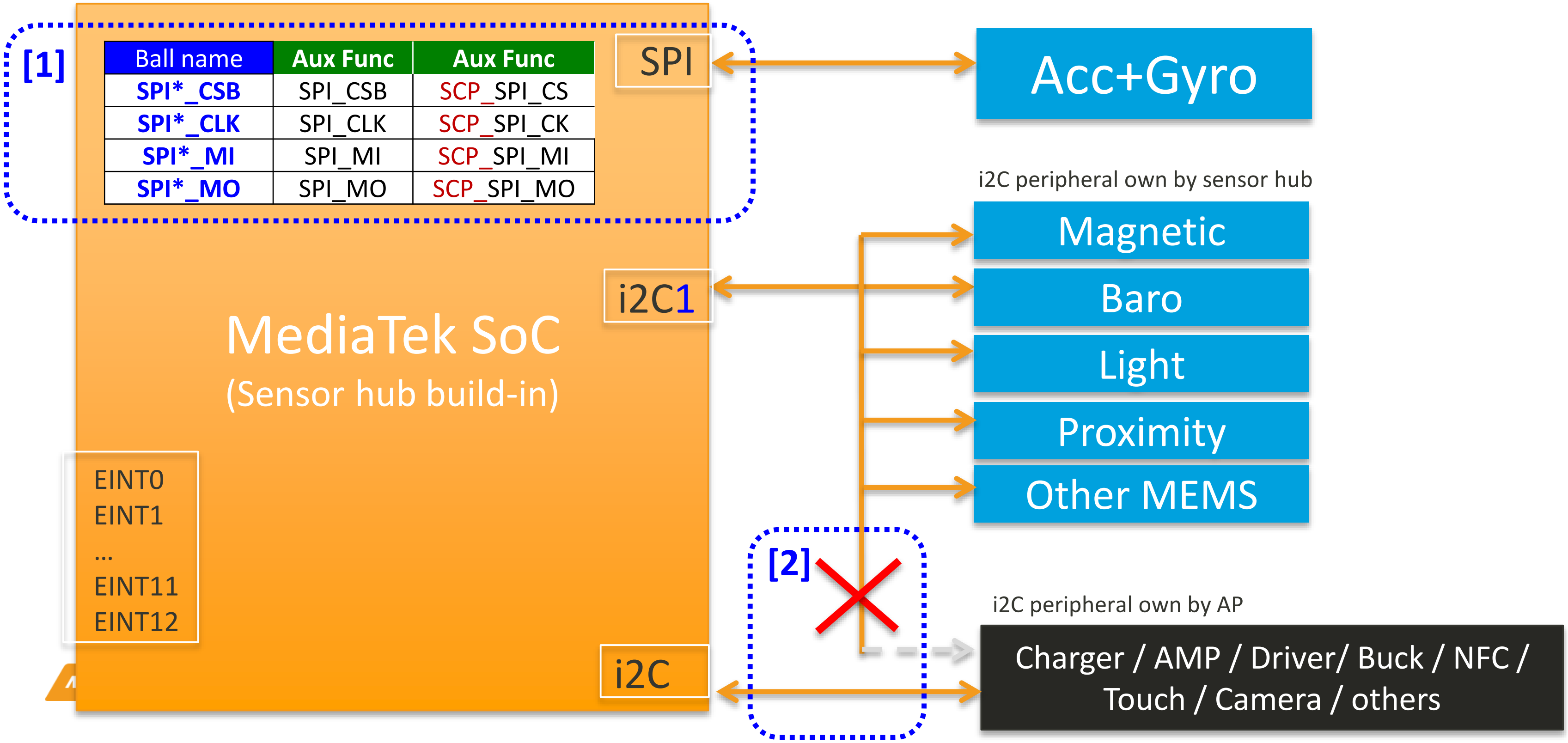


For more information about USB generic design notice, please refer to DMS

(..\HW (For Customer Release) \ Common Design Notes \ USB)

MEMS Sensor interface connection

- Accelermeter + Gyroscope : **SPI 4-wire**
  - Select correct ASIC's SPI pin that can switch between AP and SCP [1]
- Magnetic/Baro/Light/Proximity/Humidty Sensors : **i2C1**
  - **No share i2C bus** with other non-SCP device [2]
- Interrupt pin of MEMS sensor must be assign to ball **EINT[12:0]**



Ball name	Aux Func	Aux Func
SPI*_CSB	SPI_CSB	SCP_SPI_CS
SPI*_CLK	SPI_CLK	SCP_SPI_CK
SPI*_MI	SPI_MI	SCP_SPI_MI
SPI*_MO	SPI_MO	SCP_SPI_MO

MEMS Sensor Selection Notice

- **Android Compatibility Definition Document**
  - https://source.android.com/compatibility/cdd
  - Choose sensor that compatible with Android CDD
- **A+G feature notice**
  - Suggest choose sensor with : "FIFO watermark interrupt", otherwise Hifi-sensor, daydream VR will not be supported. And Sensor-location accuracy will become worse.

WaterM	FIFO watermark status. The watermark is set through bits FTH_[7:0] in *FIFO_CTRL1 (06h)*. Default value: 0 (0: FIFO filling is lower than watermark level[1]; 1: FIFO filling is equal to or higher than the watermark level)

Snapshot from
ST / LSM6DS3-C datasheet

In addition to that the common interrupts for accelerometer and gyroscope are

- **Data ready ("new-data")** for synchronizing sensor data read-out with the MCU / host controller
- **FIFO full / FIFO watermark** allows FIFO fill level and overflow handling.

Snapshot from
Bosch / BMI160 datasheet

- **additional software feature**
  - MPE (Mems Positioning Engine)
    - Required for Gyro sensor
    - For Acc+Gyro parameters, please refer page "MPE Sensor Selection Guide"
  - LPPe (LTE Position Protocol extension, Must for North America Operator)
    - Required for Baro/Pressure sensor, absolute accuracy within +/- 1hPa

MEMS Sensor Placement Notice (1/5)

- **PCB placement guidelines of Accelerometer/Gyroscope**
  - Keep a minimum distance of 20mm from components to heat source (eg: CPU, PMIC, Charger, Power Amplifier)
  - Keep away as far as possible from components to mechanical stress (eg: anchor point, screw hole, other assembly/housing stress)

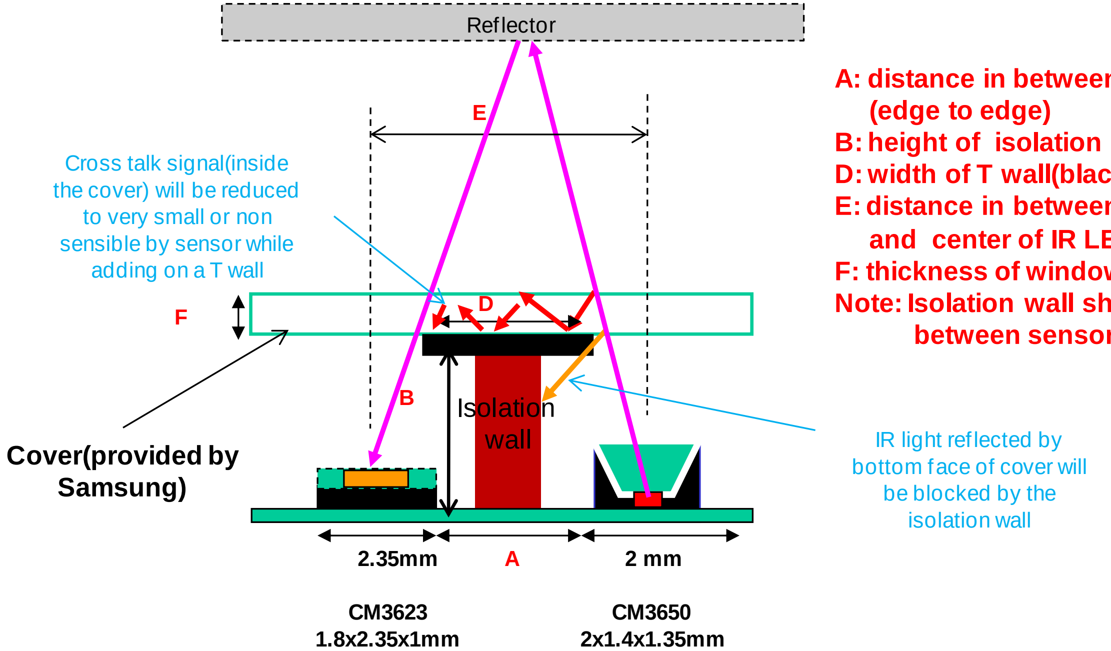
MEMS Sensor Placement Notice (2/5)

- **PCB placement guidelines of Magnetometer**
  - Keep a minimum distance of 15mm from the components to magnet, e.g. mic, speaker, vibrator, transformer, magnetic switch, etc.
  - Keep a minimum distance of 15mm from the components to magnet-conductive material (Iron, Cobalt, Nickel). They can be:
    1. Memory/SIM card socket, metal connector, screw, nut, spring
    2. IC with lead frame, battery, SAW filter, antenna, power amplifier, inductor
    3. EMI shielding case, LCD rear case
  - Keep a minimum distance of 15mm from power ICs or PCB traces of 100mA or longer
  - Do not cover the magnetic sensor with any material that can block the magnetic field .

MEMS Sensor Placement Notice (3/5)

- **ME design for ALS & PS**
  - Contact ALS & PS's vendor for more information.

CM3623+CM3650 ME design recommendation



A: distance in between sensor and IR LED (edge to edge)
B: height of isolation wall
D: width of T wall(black tape instead)
E: distance in between the center of sensor and center of IR LER
F: thickness of window(cover)
Note: Isolation wall should put in the middle in between sensor and IE LED

A=2 mm, B=2 mm, D=2.575mm, E=4.175mm, F<=1.4mm

To achieve max. detection performance, it is recommended that the transmittance of lens is above 55% for IR (850nm) and above 10% for visible light (550nm).

MEMS Sensor Placement Notice (4/5)

- **PCB placement guidelines for pressure sensor**
  - Keep a reasonable distance to push-button contacts, hot spots, anchor points and maximum mechanical stress point when placing the sensor device.
  - Do not position the sensor directly beneath a push-button contact.
  - Avoid total and partial covering with any protective material, such as epoxy resin.
  - Avoid underfill or cleaning material under the sensor device.

MEMS Sensor Placement Notice (5/5)

- **PCB placement guidelines for humidity sensor**
  - Create PCB slits (破孔) around sensor to prevent heat propagation by PCB.
  - Remove copper for all layers to prevent heat propagation by copper.
  - Reduce trace width to prevent heat propagation by copper.
  - Isolate sensor by ME design change to prevent heat propagation from peripheral components by Convection/Radiation.

MPE Sensor Selection Guide

- **Basic H/W requirement**
  - ✓ Support FIFO
  - ✓ Power (lower is better)

- **Pass Android HiFi CTS 7.0 : Performance will be downgraded if CTS failed**

Not suggest

	Parameter	HiFi VR requirement	MPE requirement	BMI160	ICM20690	LSM6DS3TR-C	ICM20608D
	Accelerometer						
A+G Sensor	Sensitivity error (TYP.)		1%	1%	1%	1%	2%
	Clock freq. (ODR) error	400Hz with <0.1% jitter	200Hz, 1% clock error	1%	1% (gyro active) 3% (acc only)	1%	1% (gyro active) 5% (acc only)
	Noise Density	400 µg/√ Hz	200 µg/√ Hz	180 ug/√Hz	100µg/√Hz	90 µg/√ Hz @ FS = +/- 2,4,8 g 130 µg/√ Hz @ FS = +/- 16 g	250µg/√ Hz
	Bias Change vs Temperature	± 1mg/C	± 1mg/C	± 1 mg/k	X/Y axis +/- 0.5mg/c Z axis 1mg/c	± 0.5 mg/ °C	X/Y axis +/- 0.5mg/c Z axis 1mg/c
	Best-fit line non linearity	0.50%	0.50%	± 0.3%	± 0.3%	± 0.3%	± 0.5%
	Sensitivity change vs Temperature	0.03% / C	0.03% / C	± 0.03%/k	± 0.008%/k	±0.01% (from -40° to +85°)	0.016 % / °C
	Gyroscope						
	Sensitivity error (TYP.)		1%	1%	1%	±1%	2%
	Clock freq. (ODR) error	400Hz with <0.1% jitter	200Hz, 1% clock error	1%	1% (gyro active) 3% (acc only)	2%	1% (gyro active) 5% (acc only)
	Noise Density	0.007 °/s/√ Hz	0.007 °/s/√ Hz	0.007 dps/√Hz	0.004 °/s/√ Hz	5 mdps/√ Hz	0.008 °/s/√ Hz
	Bias Change vs Temperature	± 0.05°/ s / °C	± 0.05°/ s / °C	± 0.05 dps/k	± 0.02dps/c	± 0.015 dps /°C	± 0.1dps/c
	Best-fit line non linearity	0.20%	0.20%	0.001	± 0.1%	± 0.1%	± 0.1%
	Sensitivity change vs Temperature	0.02% / C	0.02% / C	± 0.02%/k	± 0.016%/k	±0.007% (from -40° to +85°)	± 0.024%

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